

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Satna Rosa Platform

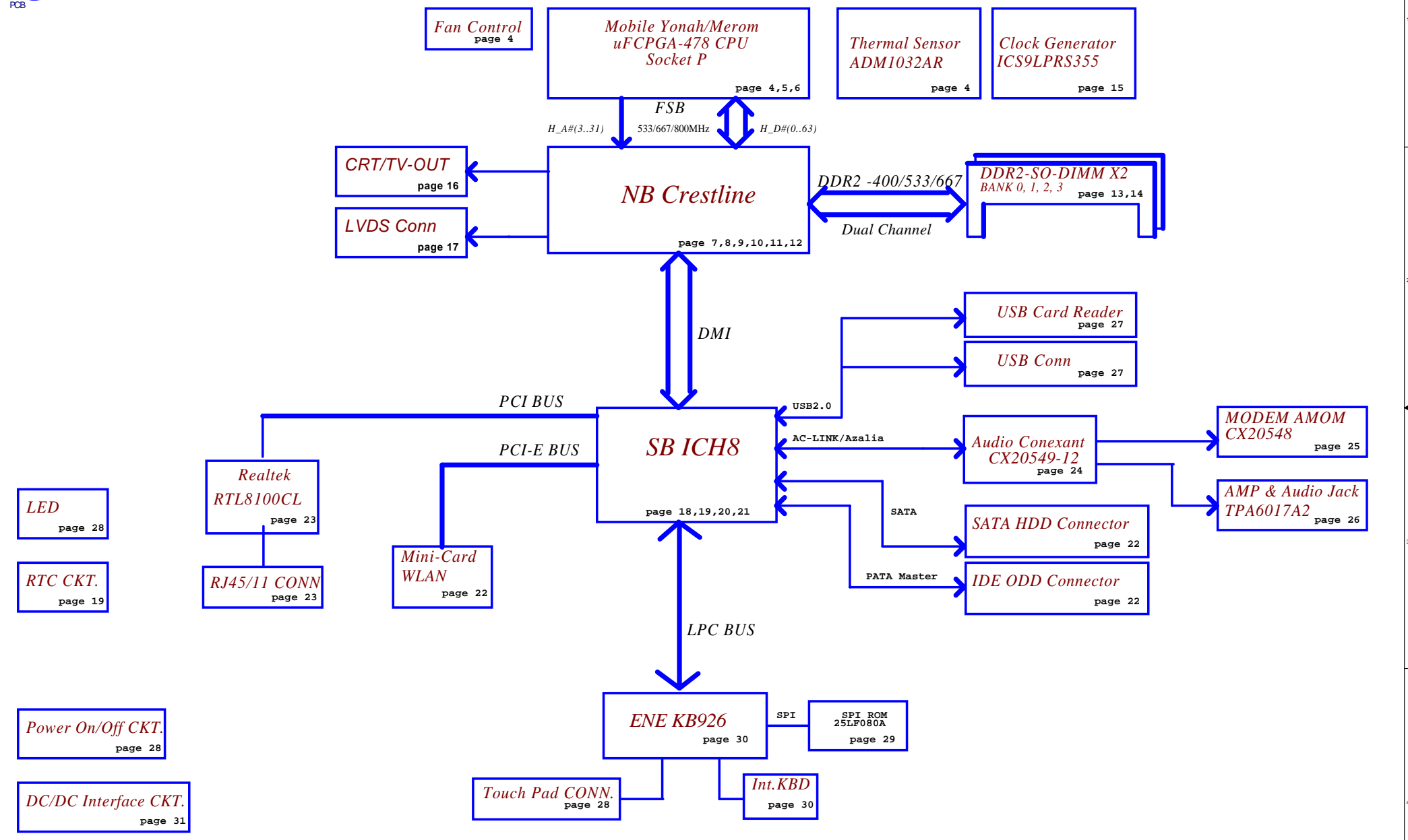
2007-05-29

REV:1.0

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Spartan 1.0 (Merom +Crestline+ICH8)

ZZZ1
PCB



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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD22	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

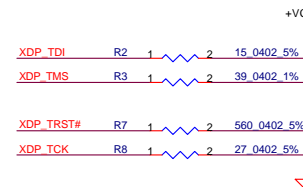
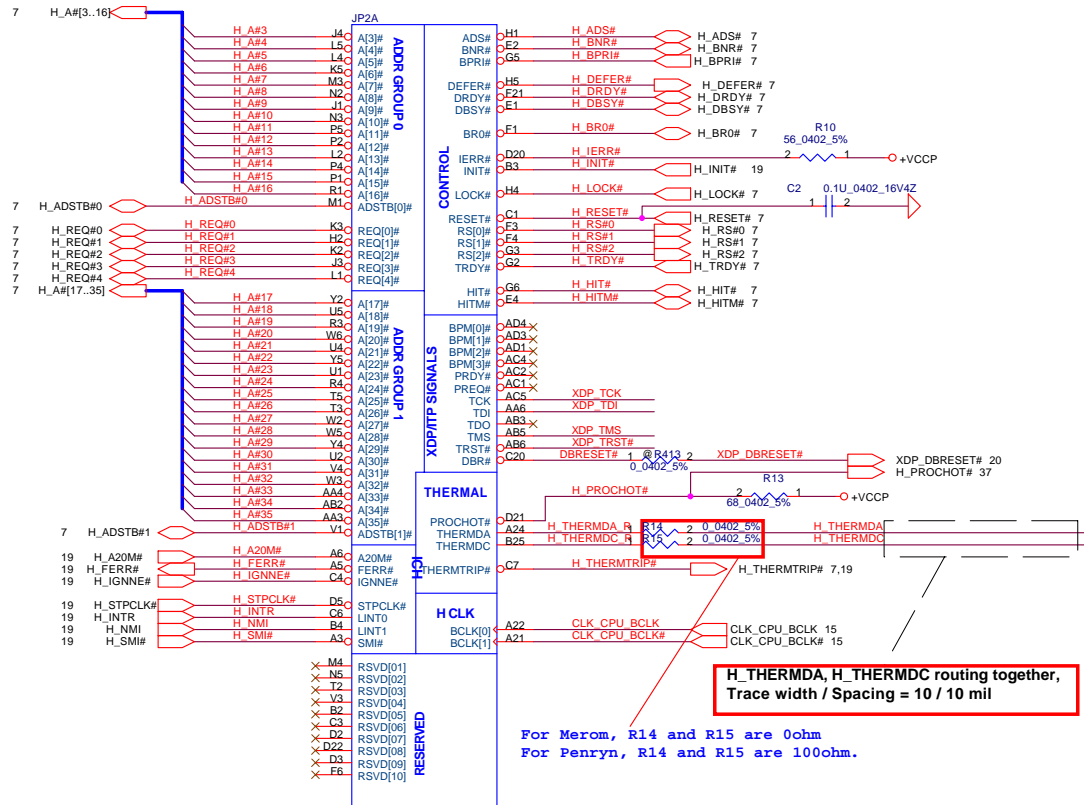
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

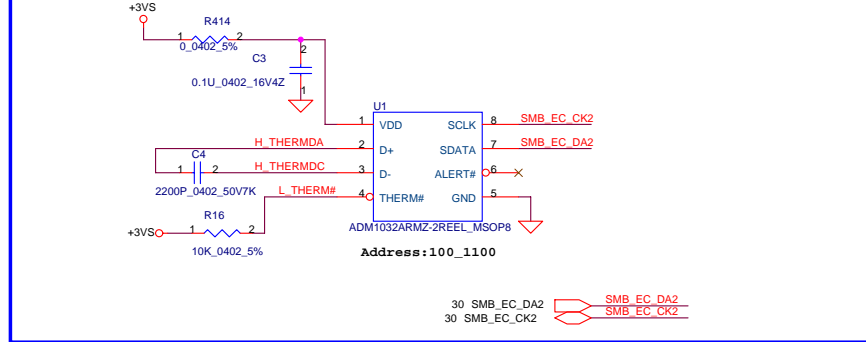
BOM: 43148632L01(965GM) & 43148632L02(960GML)

Jump-Short: PJP?

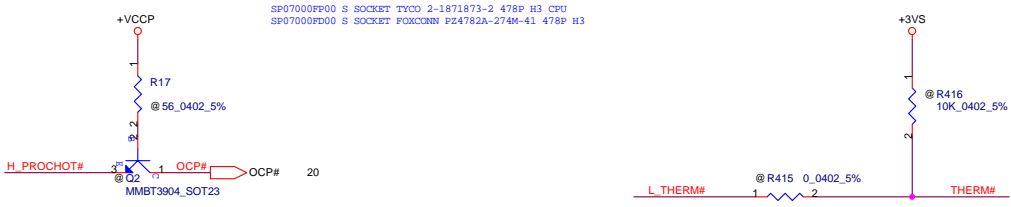
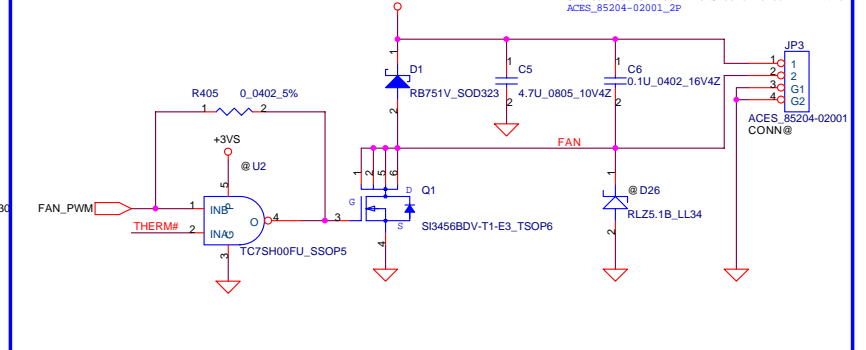
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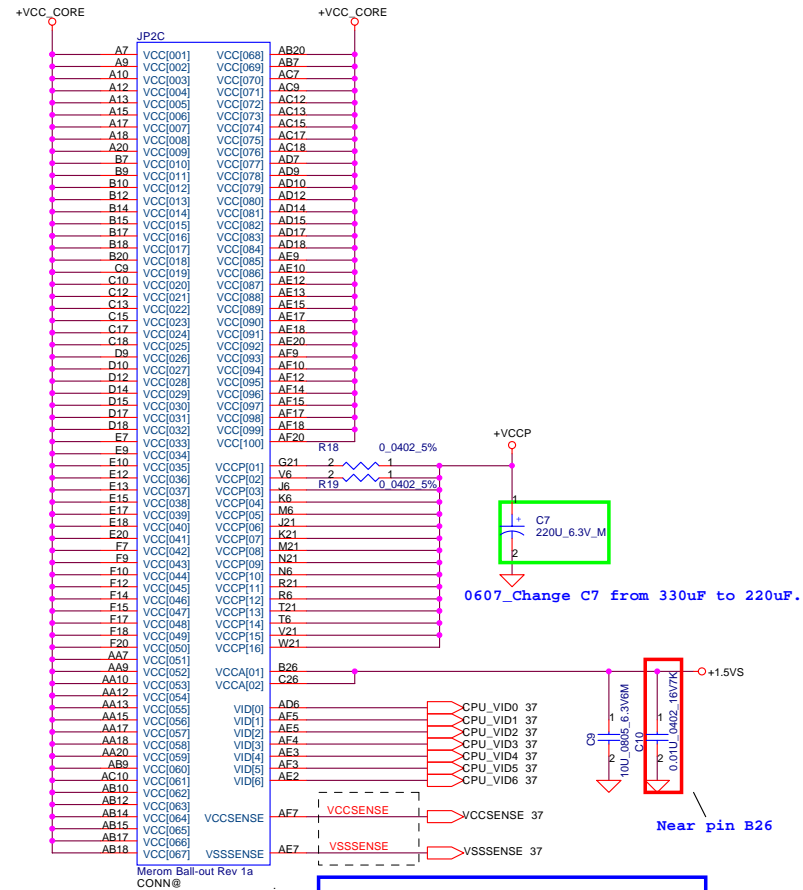
Thermal Sensor ADM1032ARMZ



PWM Fan Control circuit

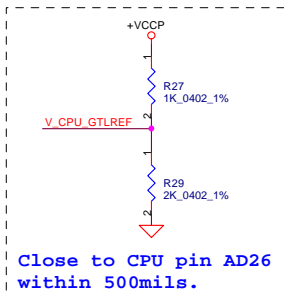


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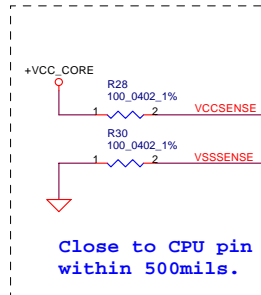


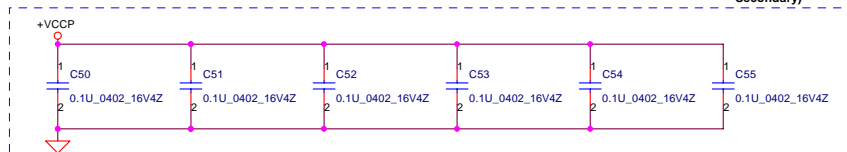
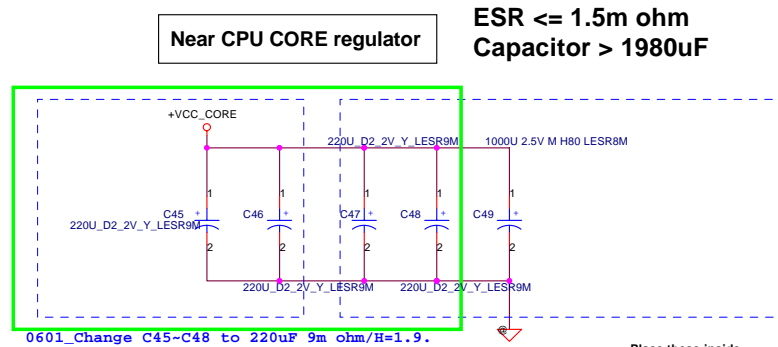
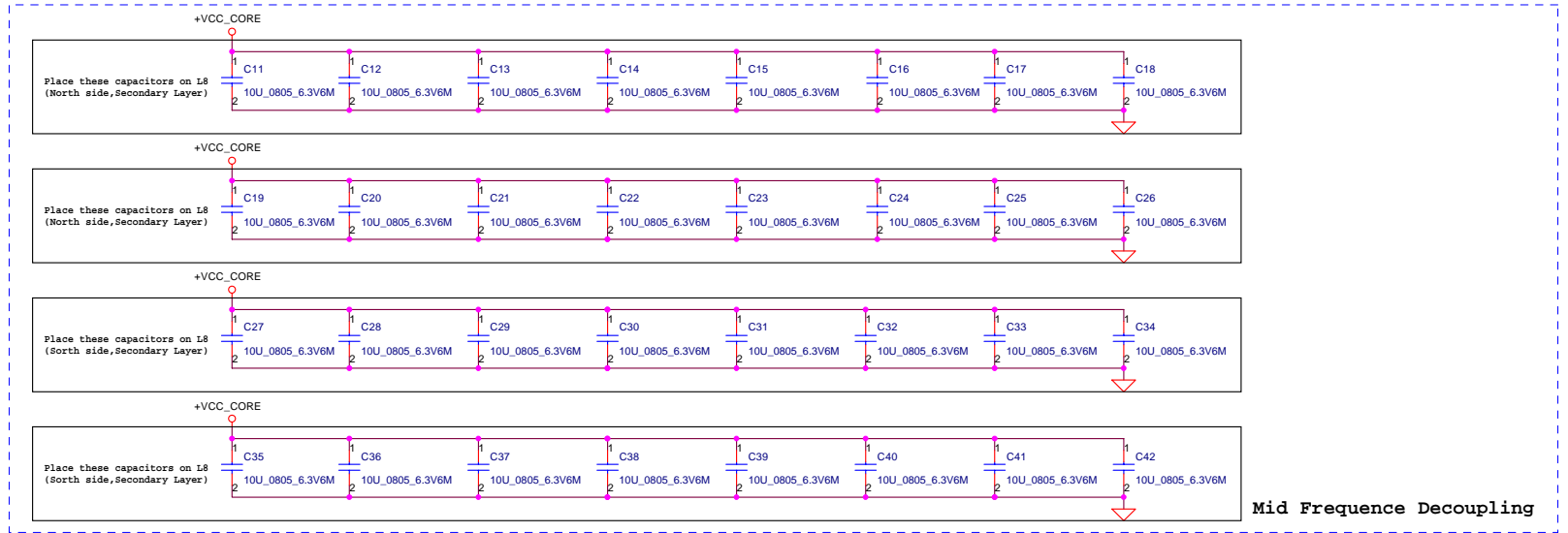
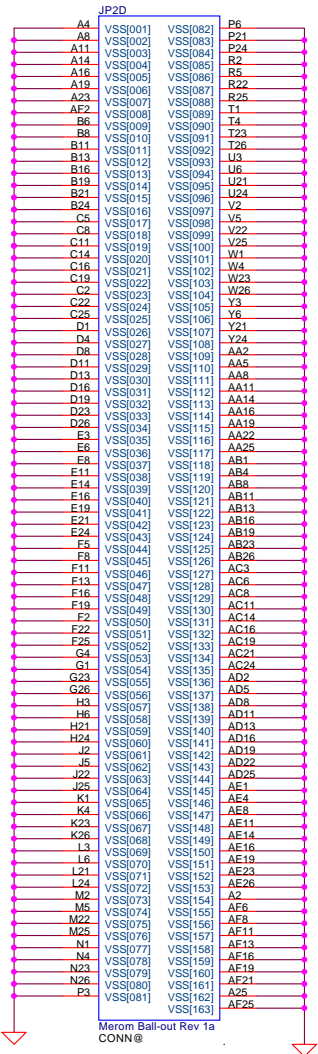
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

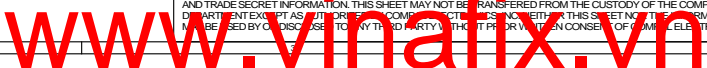


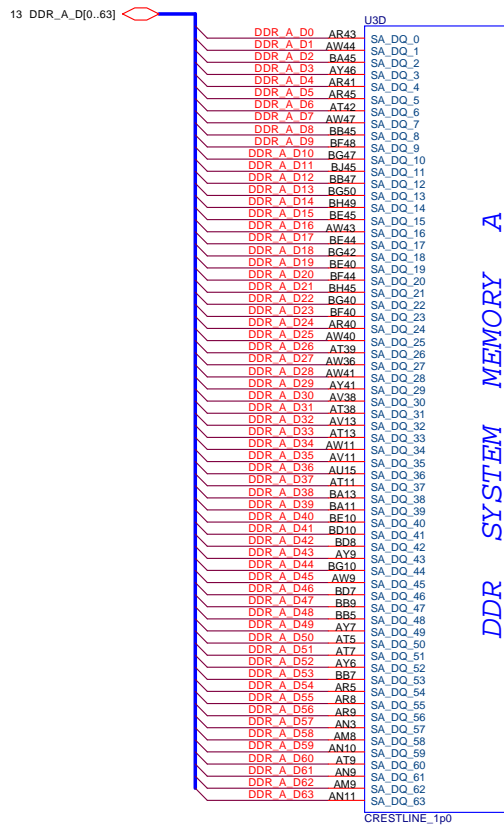
Length match within 25 mils.
The trace width/space/other is
20/7/25.



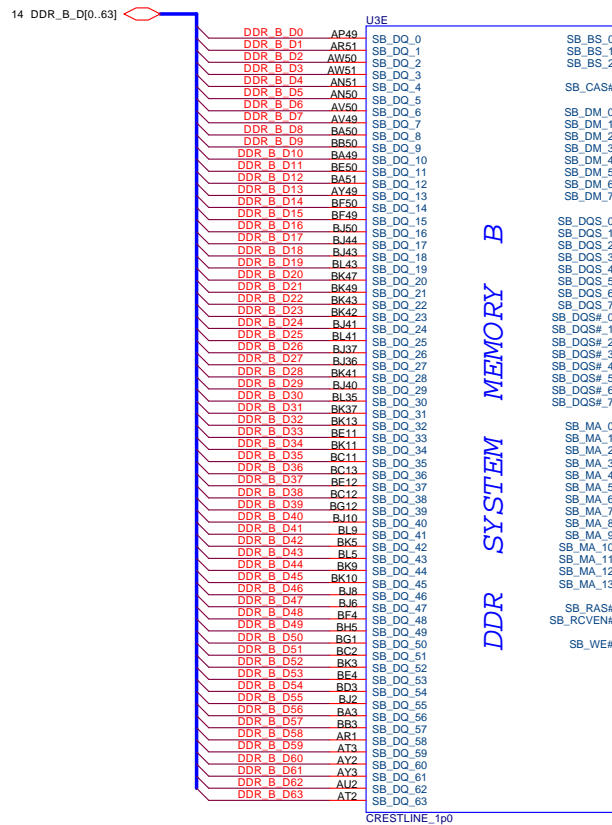


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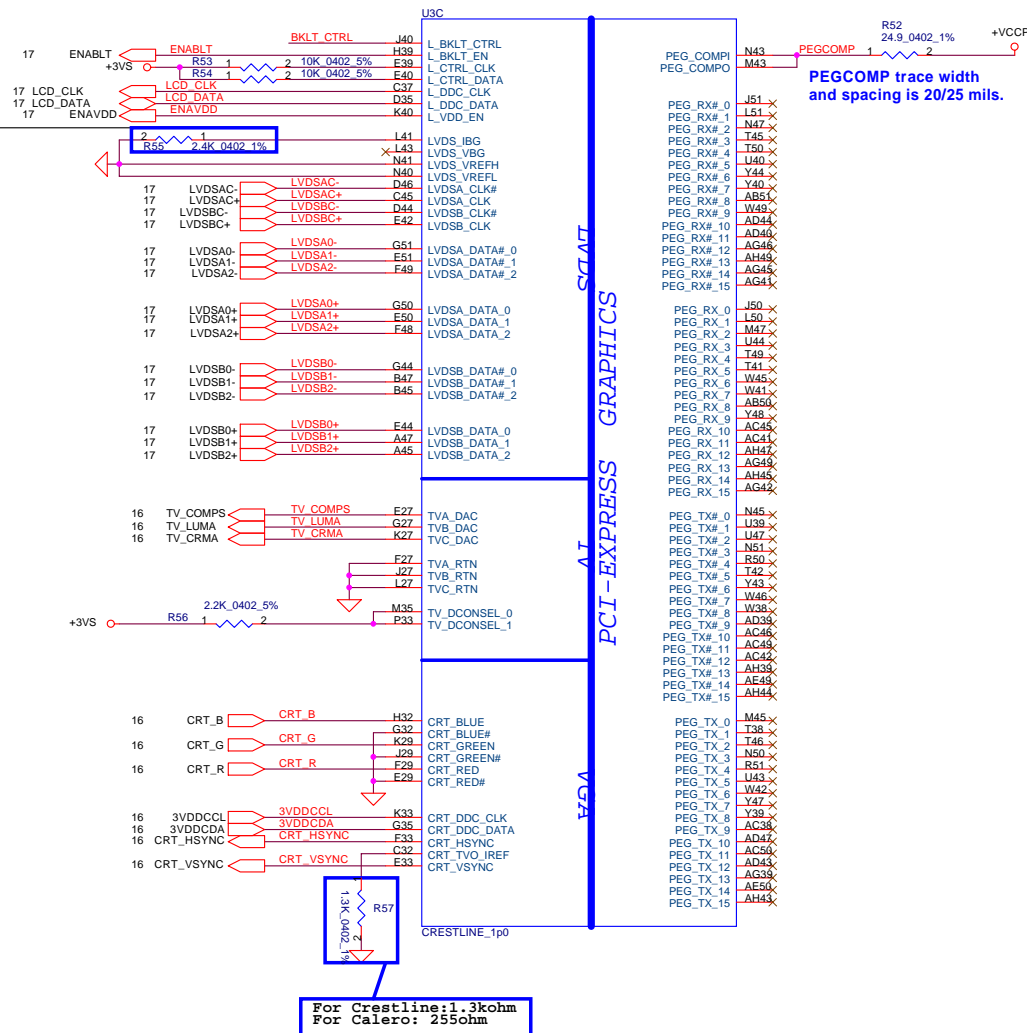
DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

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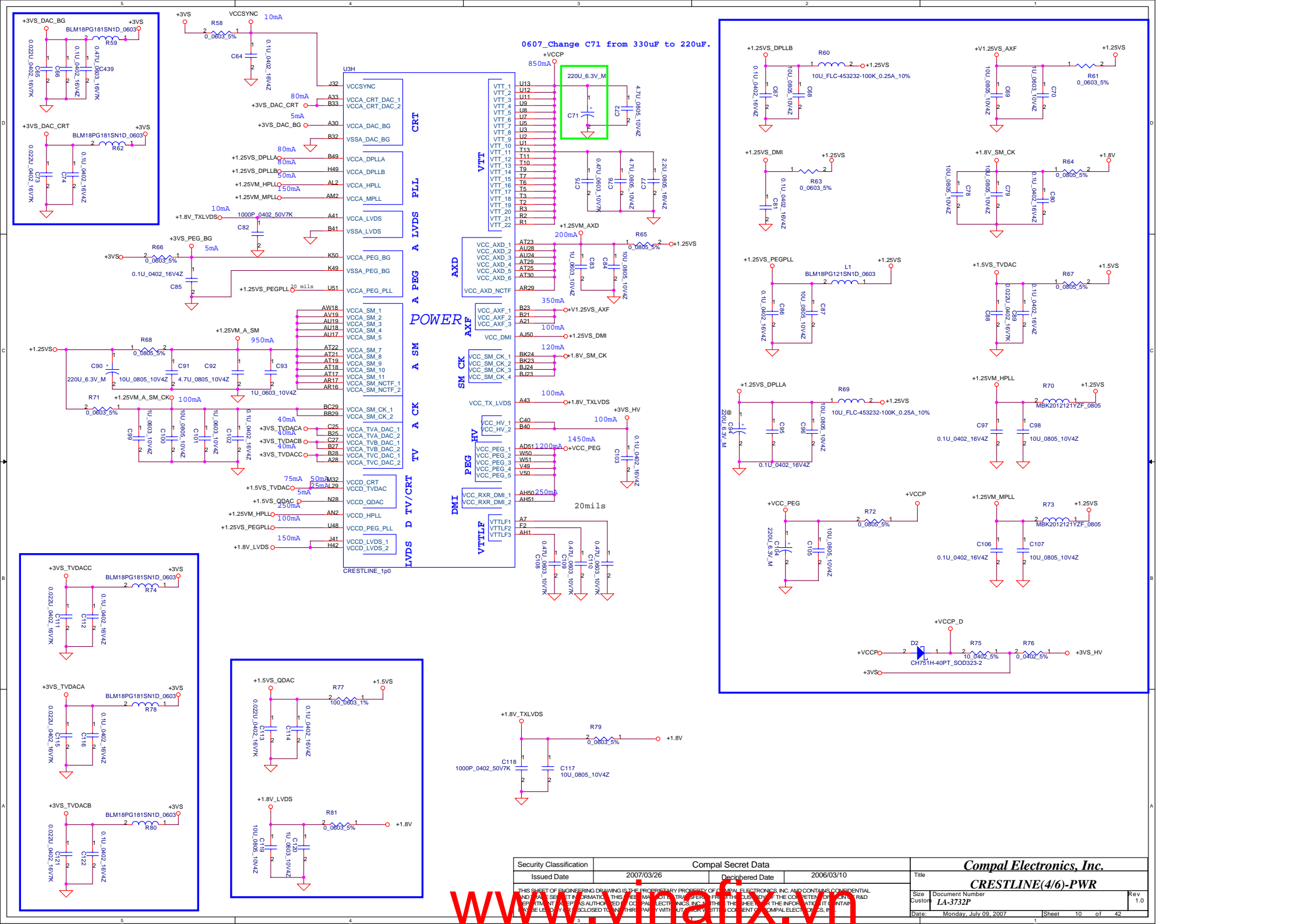
For Crestline: 2.4kohm
For Calero: 1.5kohm



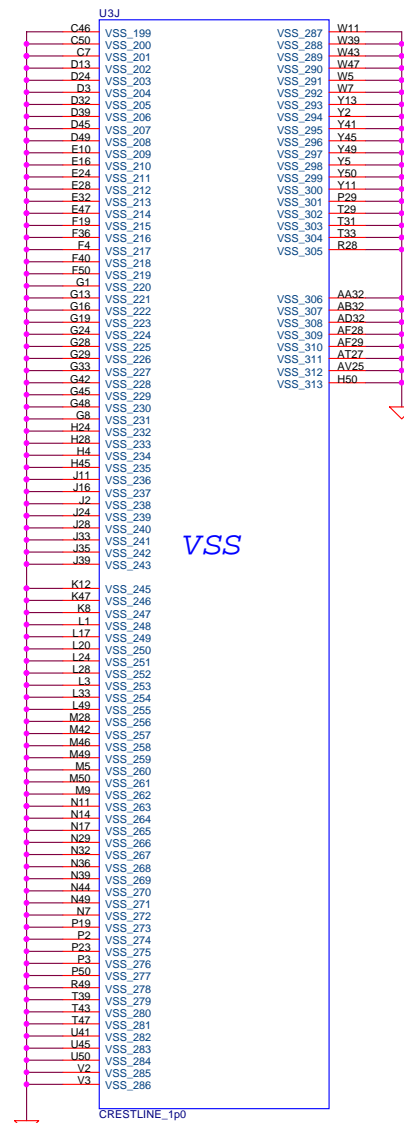
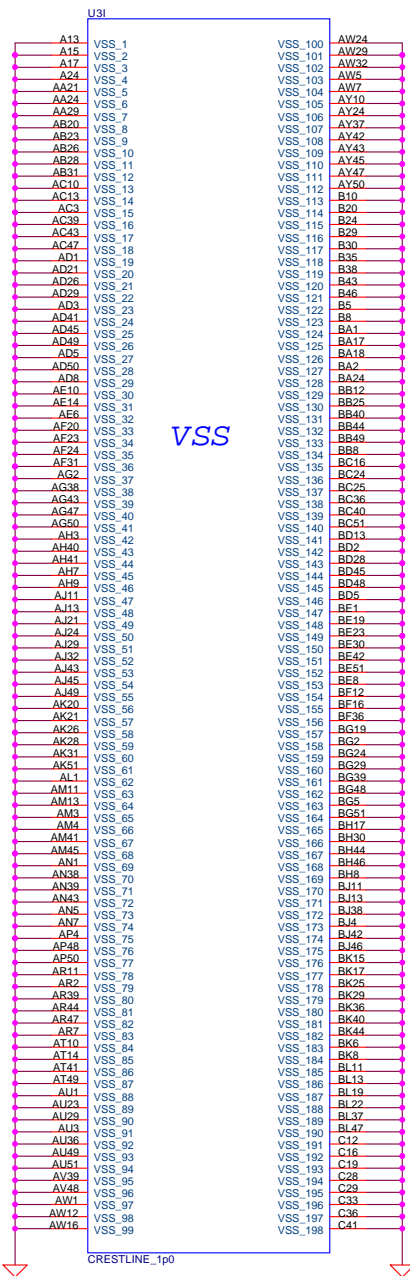
Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

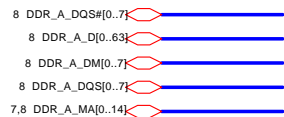
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down



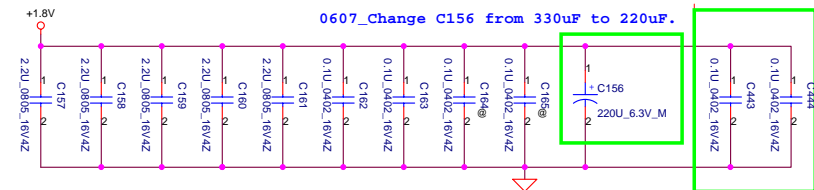
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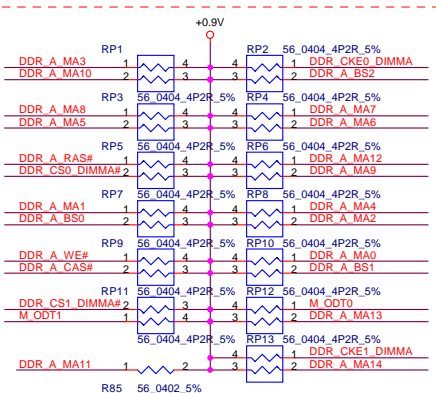
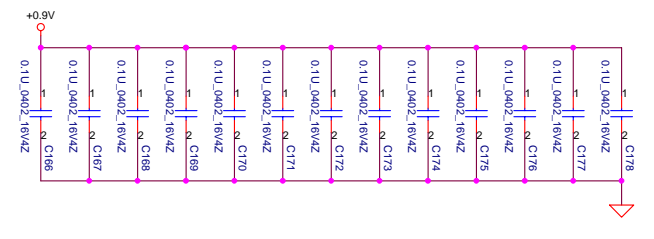


Layout Note:
Place near JP34

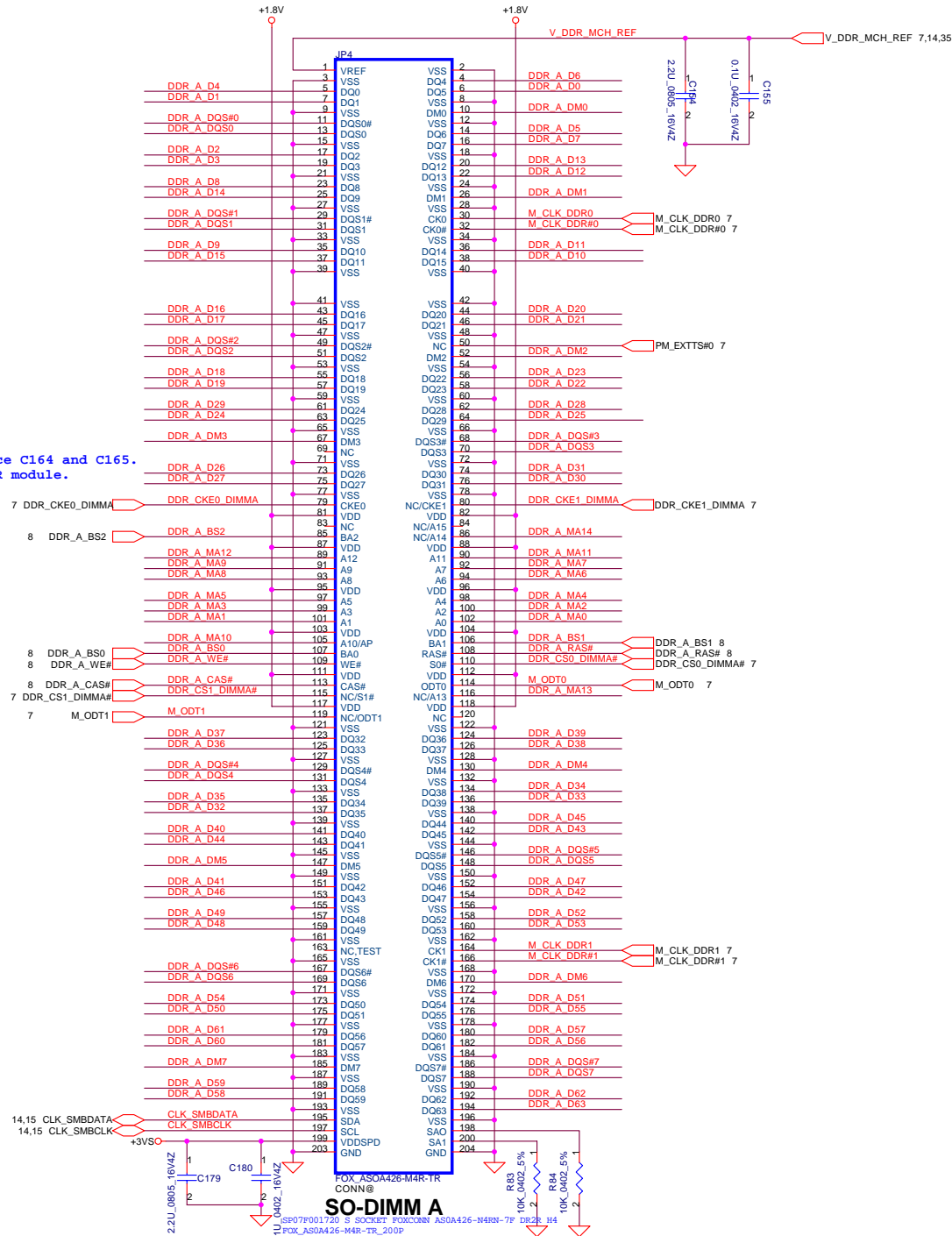


0605_Add C443 and C444 to replace C164 and C165.
To solve interfere with DDR module.

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



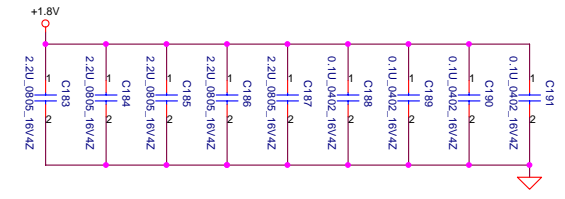
Layout Note:
Place these resistor closely JP34, all trace length Max=1.5"



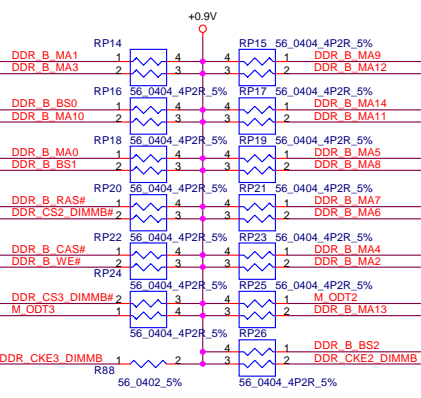
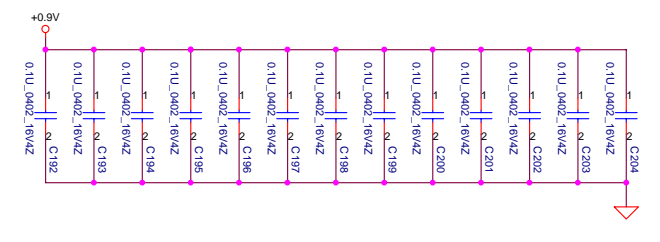
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						DDRII-SODIMM SLOT1	
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8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
7,8 DDR_B_MA[0..14]

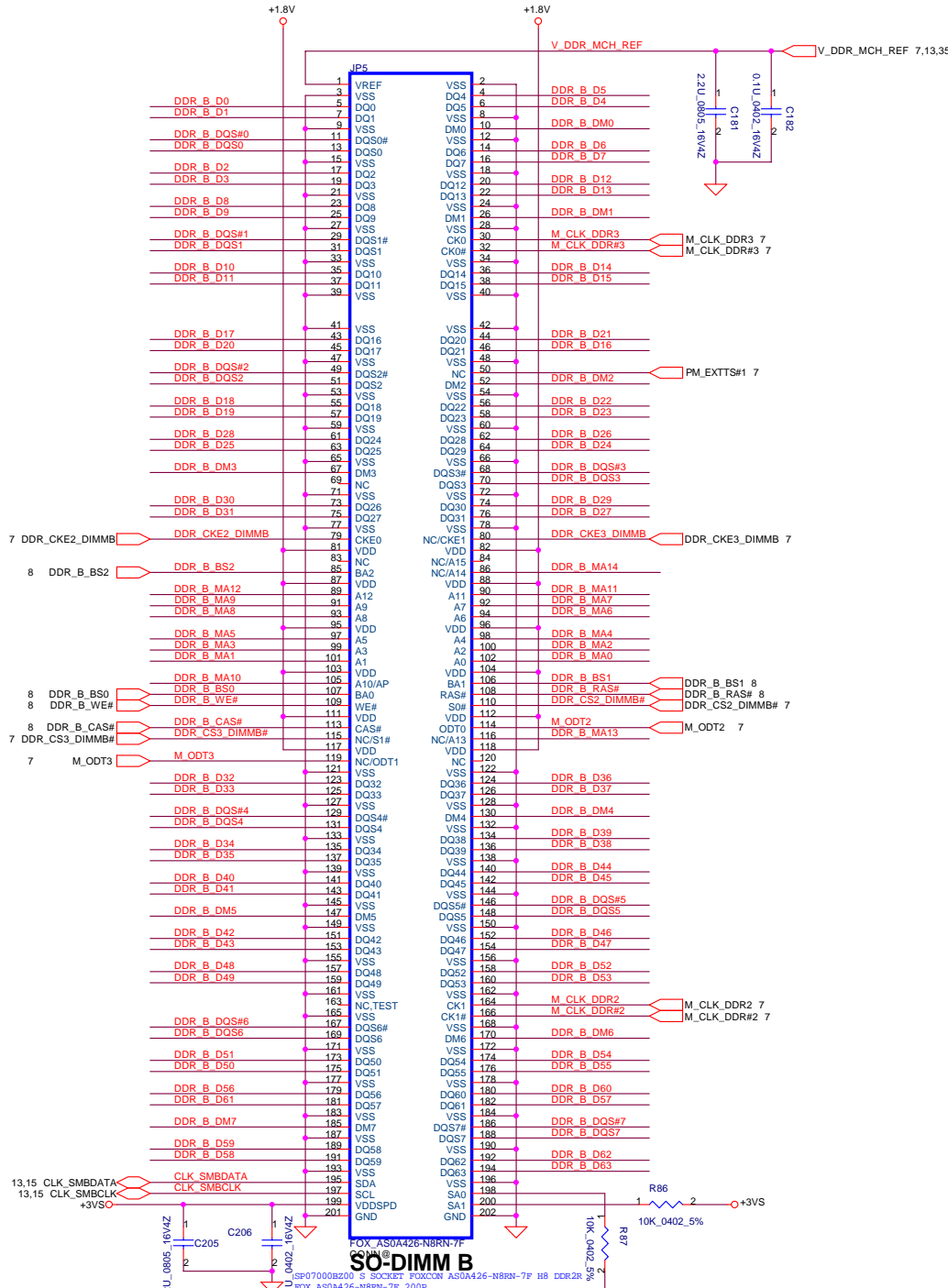
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



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				<i>DDRII-SODIMM SLOT2</i>		
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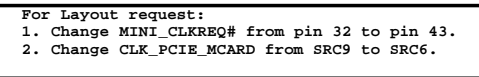
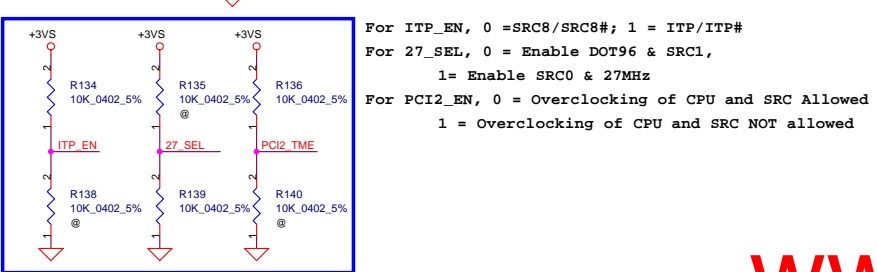
FSB Frequency Selet:

30 CLK_LPC_DEBUG @ R412
0.0402 5%
PC12 TIME
+1.25V5_CK505

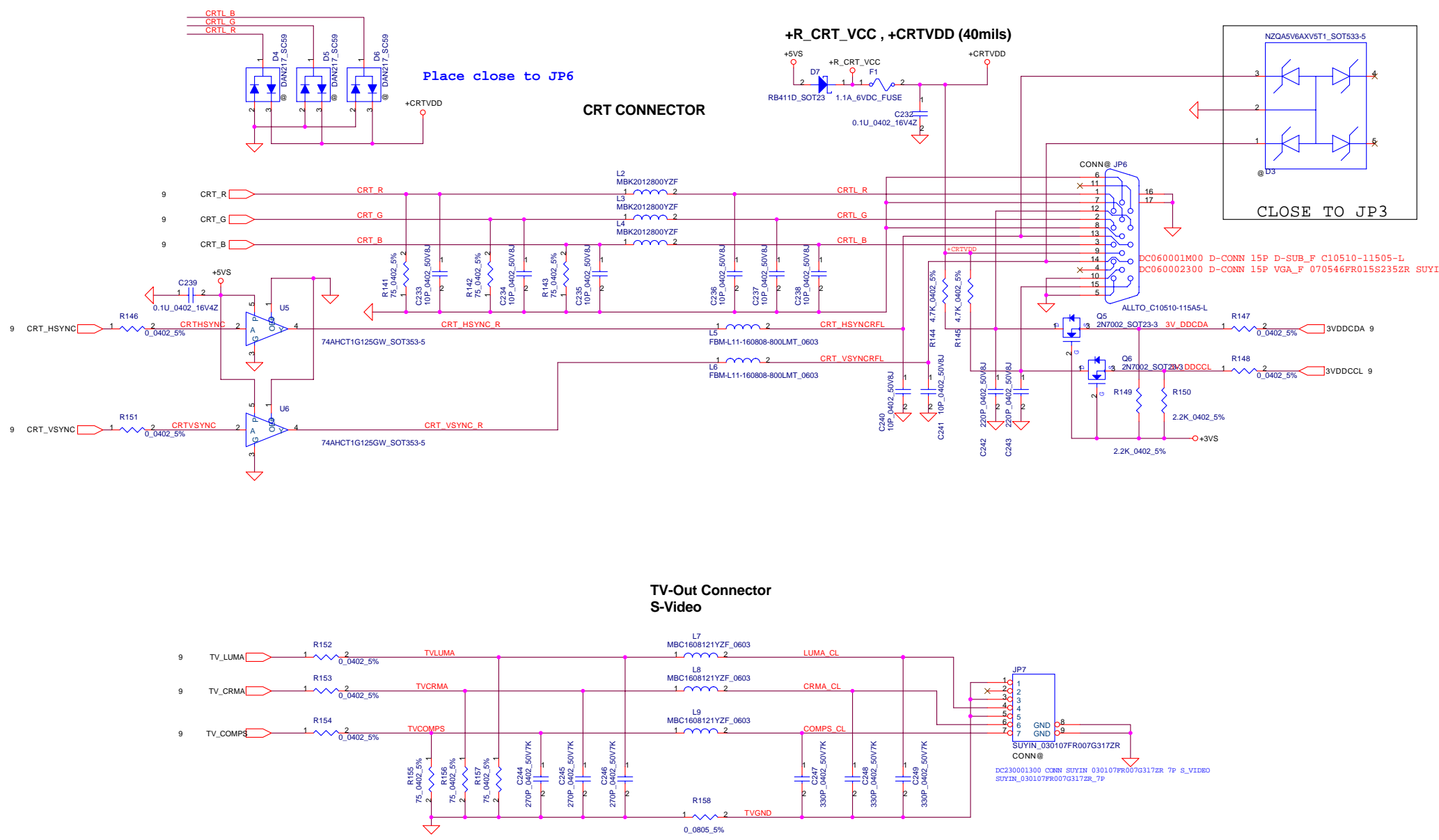
1 R93 2
56.0402 5%
CLRP1
NO SHORT PADS
VCCP

R97
2.2K 0.402 5%
FSA 2 1
MCH CLKSEL0

CLRP4, CLRP5 for 667/800 FSB select
SHORT CLRP5, NO SHORT CLRP4 -- CPU option
SHORT CLRP4, NO SHORT CLRP5 -- FSB 667

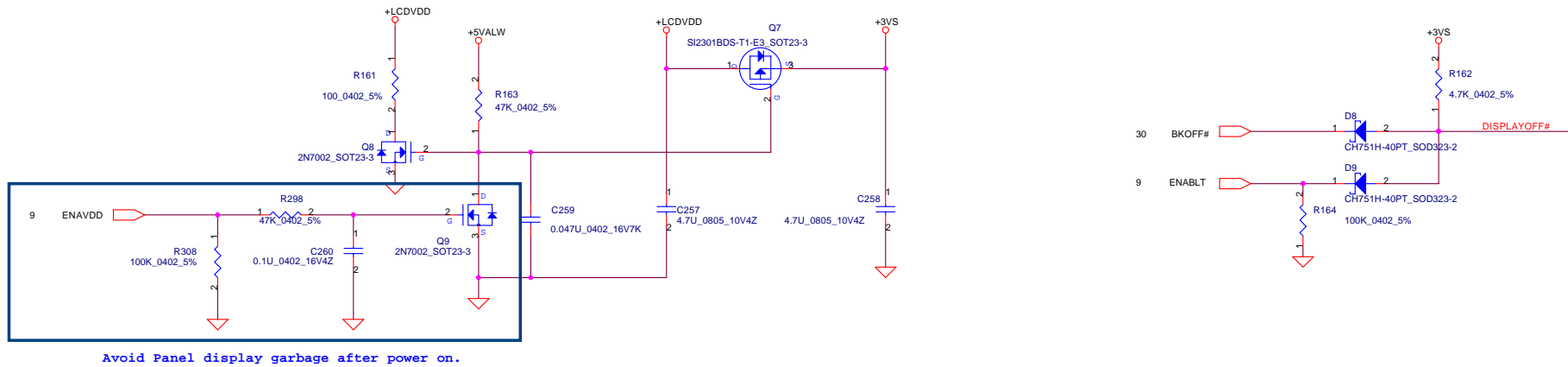
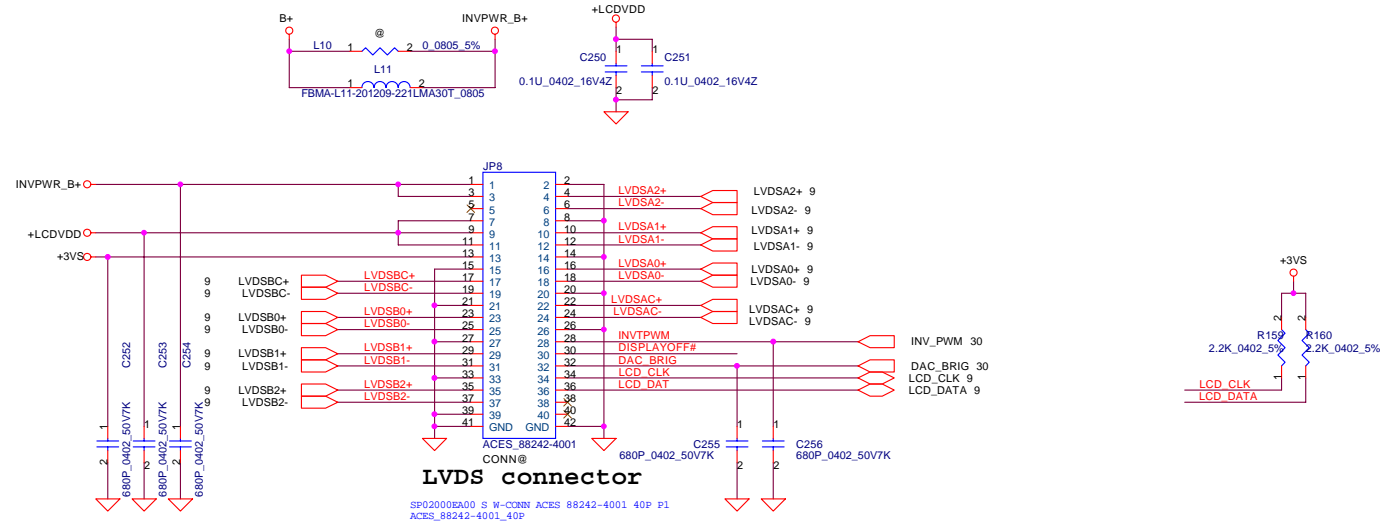


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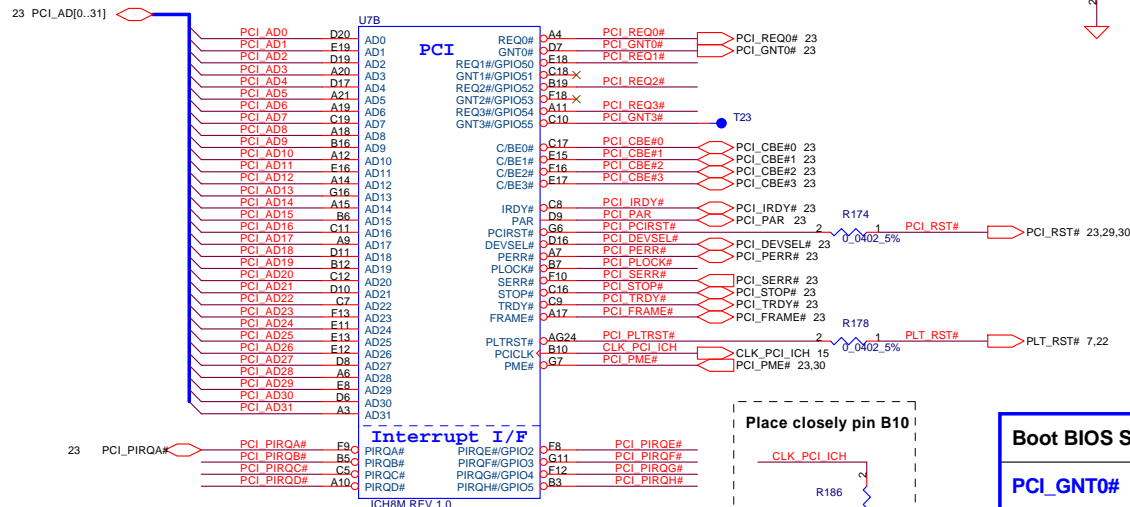
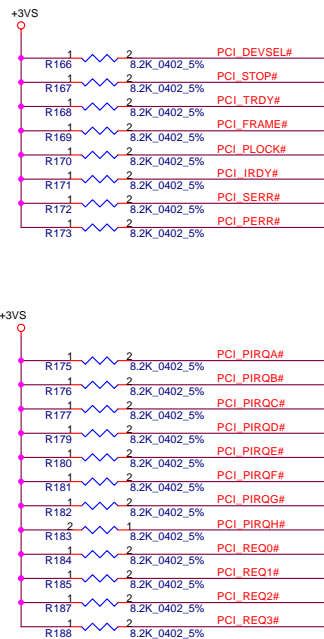
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LVDS CONN

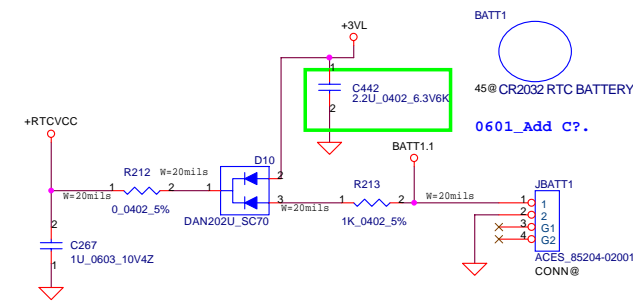
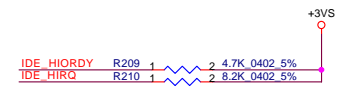
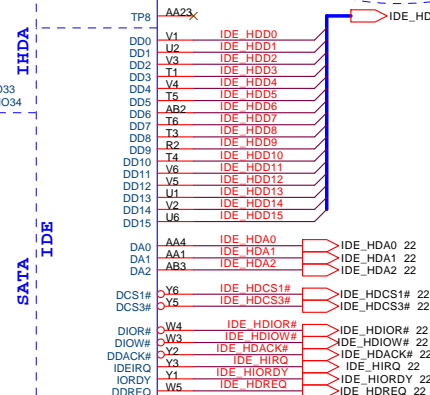
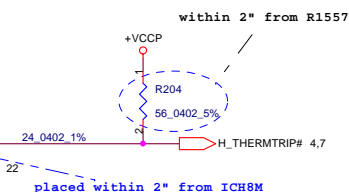
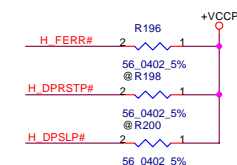
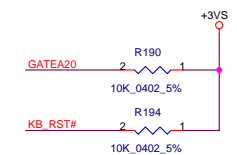


Avoid Panel display garbage after power on.

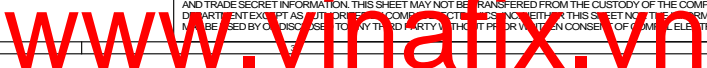
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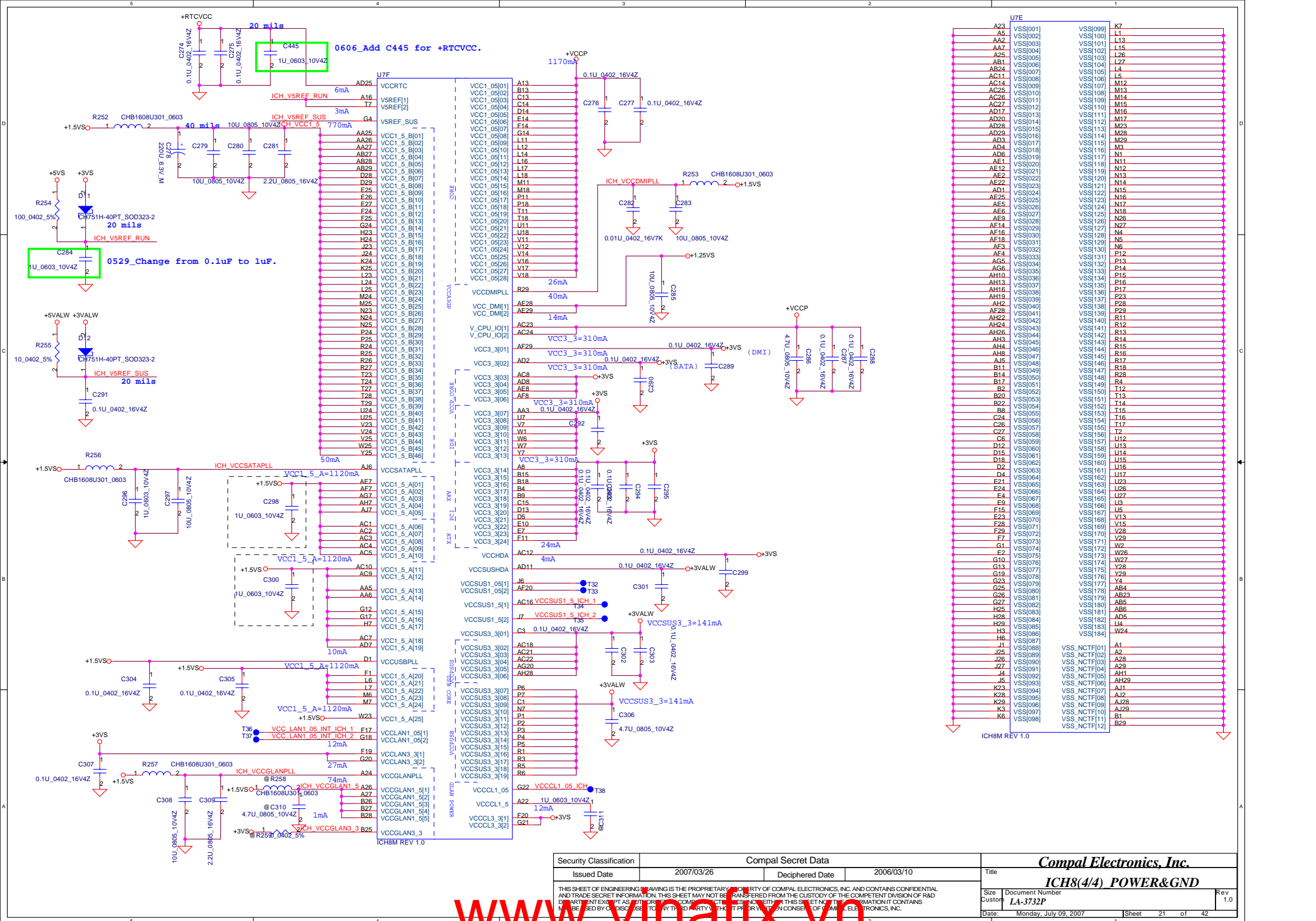


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *
A16 swap override Strap		
PCI_GNT3#	*Low= A16 swap override Enble High= Default	



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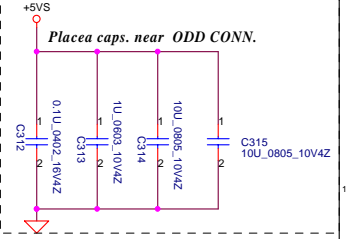
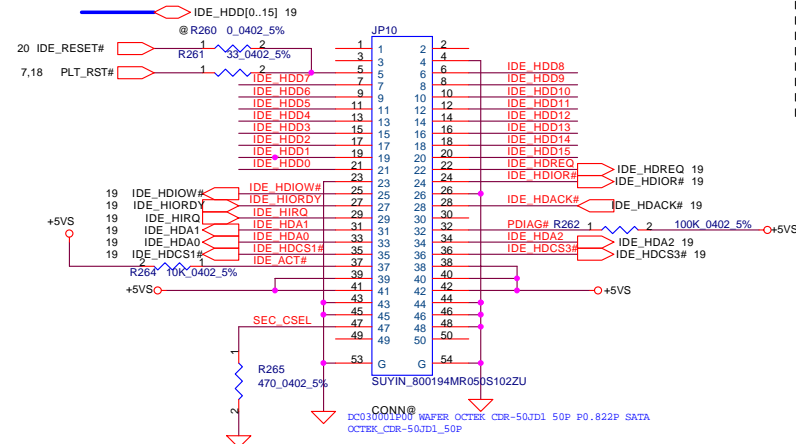
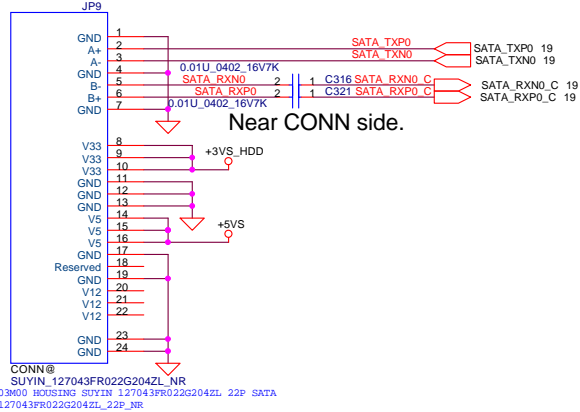
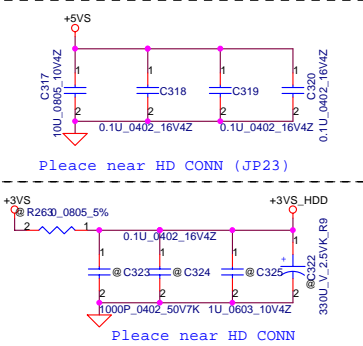




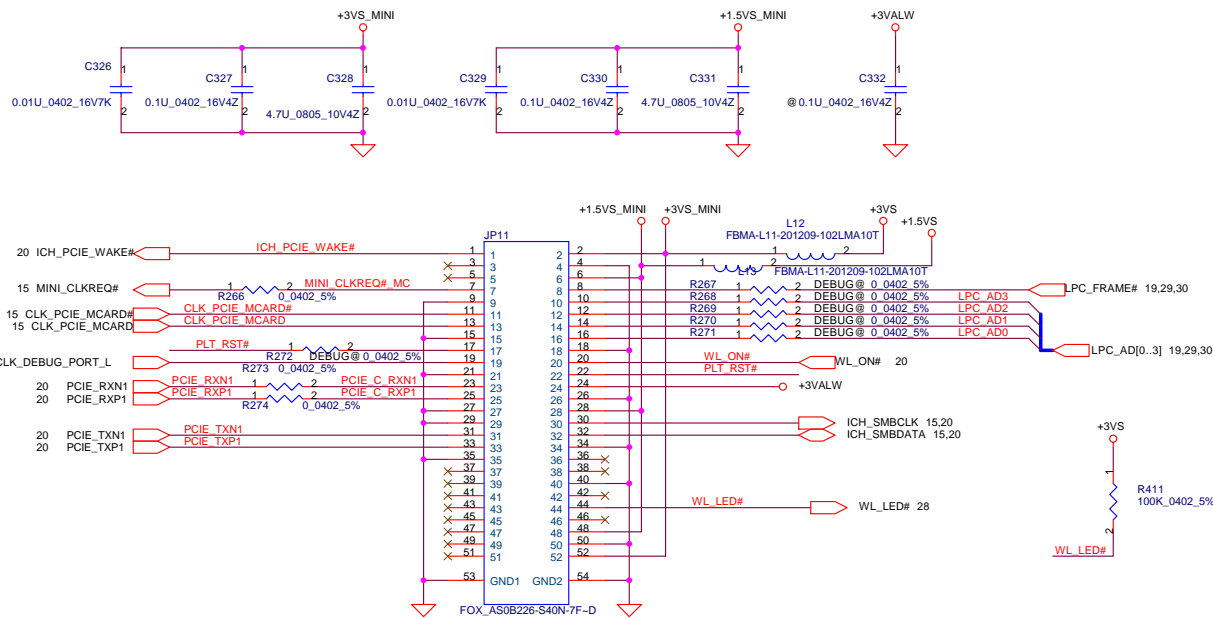
HDD Connector

CD-ROM Connector

Place caps. near ODD CONN.



Mini-Express Card---WLAN



Mini Card STANDOFF

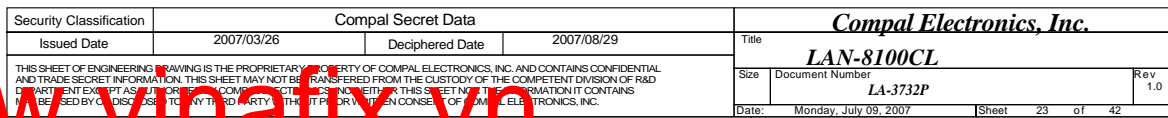


ECO29000100 MINICARD_STANDOFF_8

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Compal Electronics, Inc.			
HDD/ODD/Mini Card CONN.			
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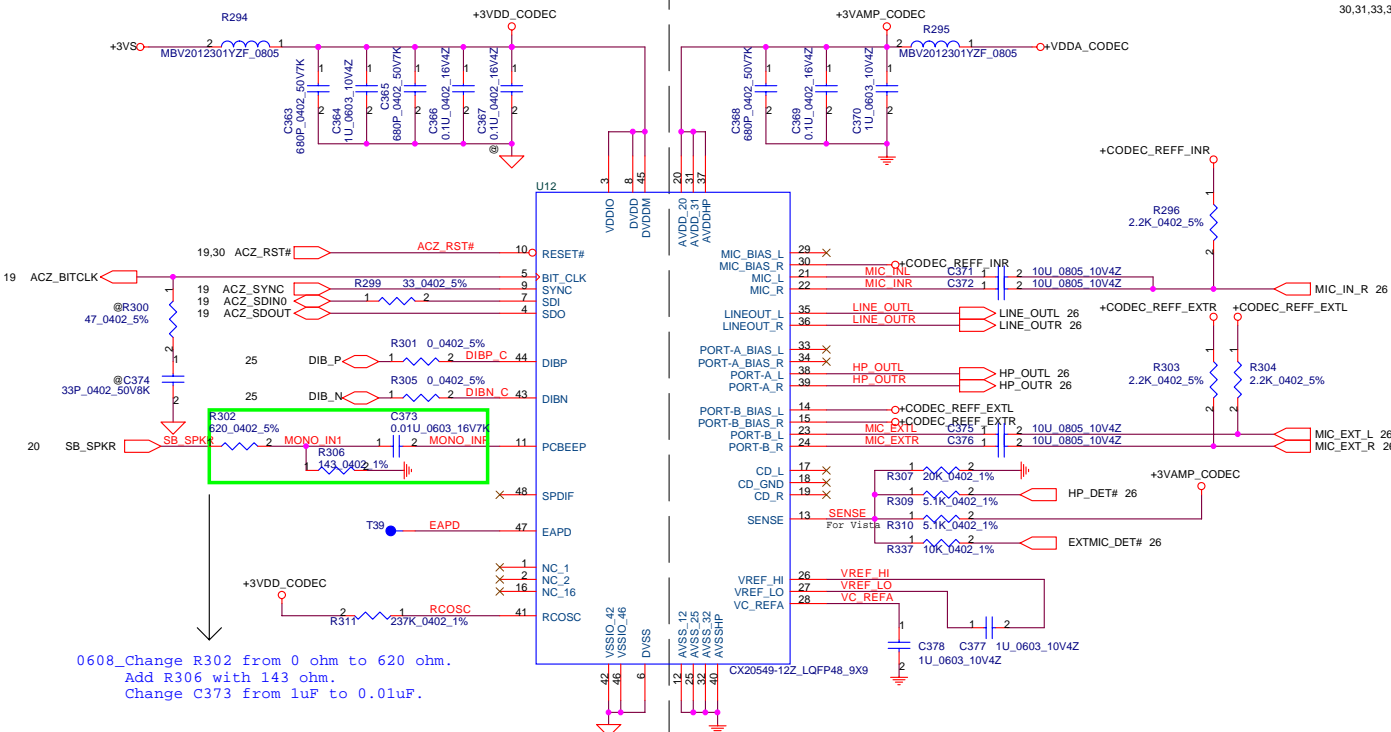
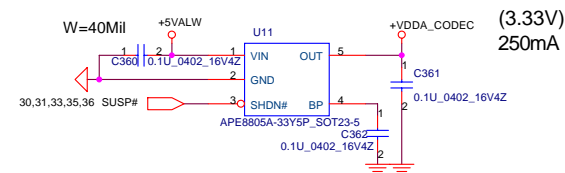


AUDIO CODEC

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

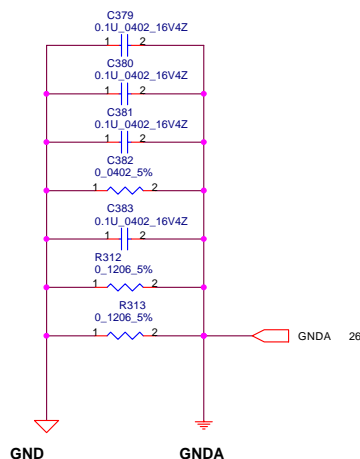
CODEC POWER



0608_Change R302 from 0 ohm to 620 ohm.
Add R306 with 143 ohm.
Change C373 from 1uF to 0.01uF.

DIGITAL

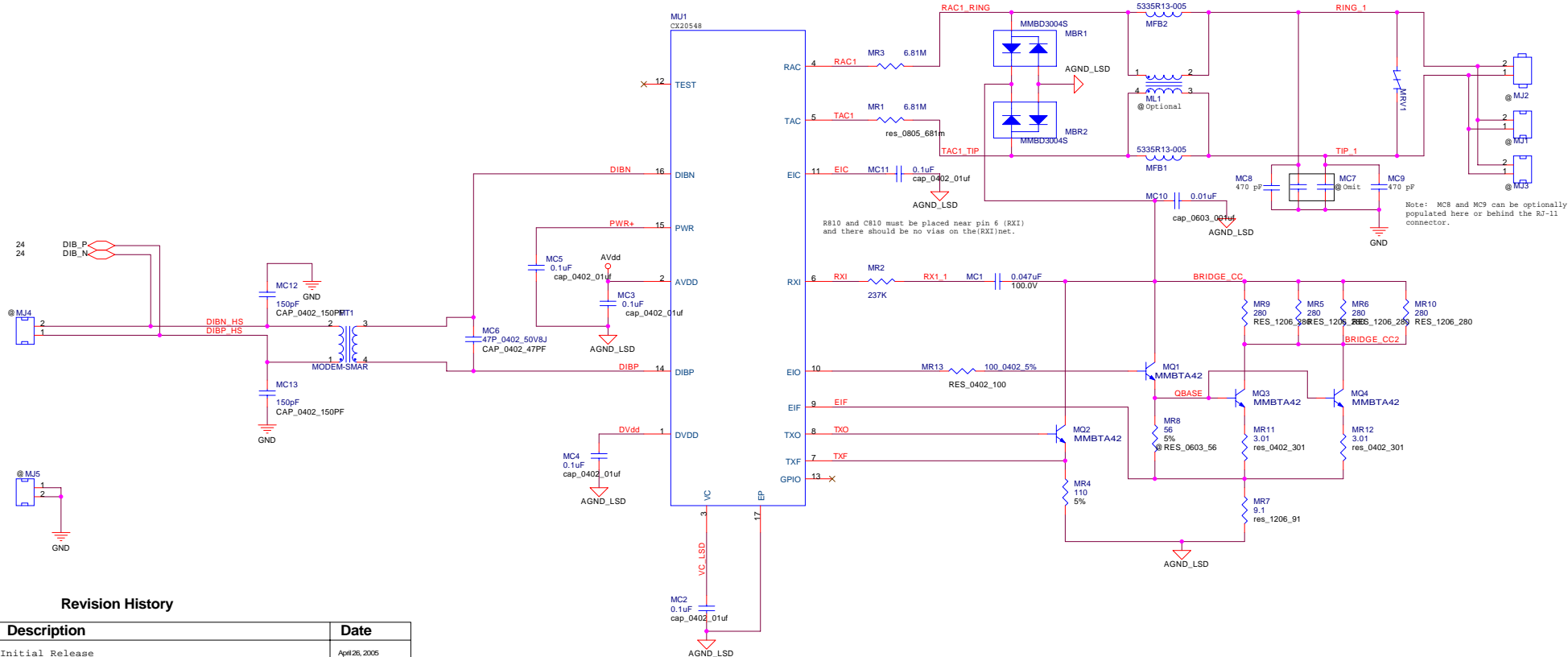
ANALOG



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

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				AMOM_codec		
				Size	Document Number	Rev
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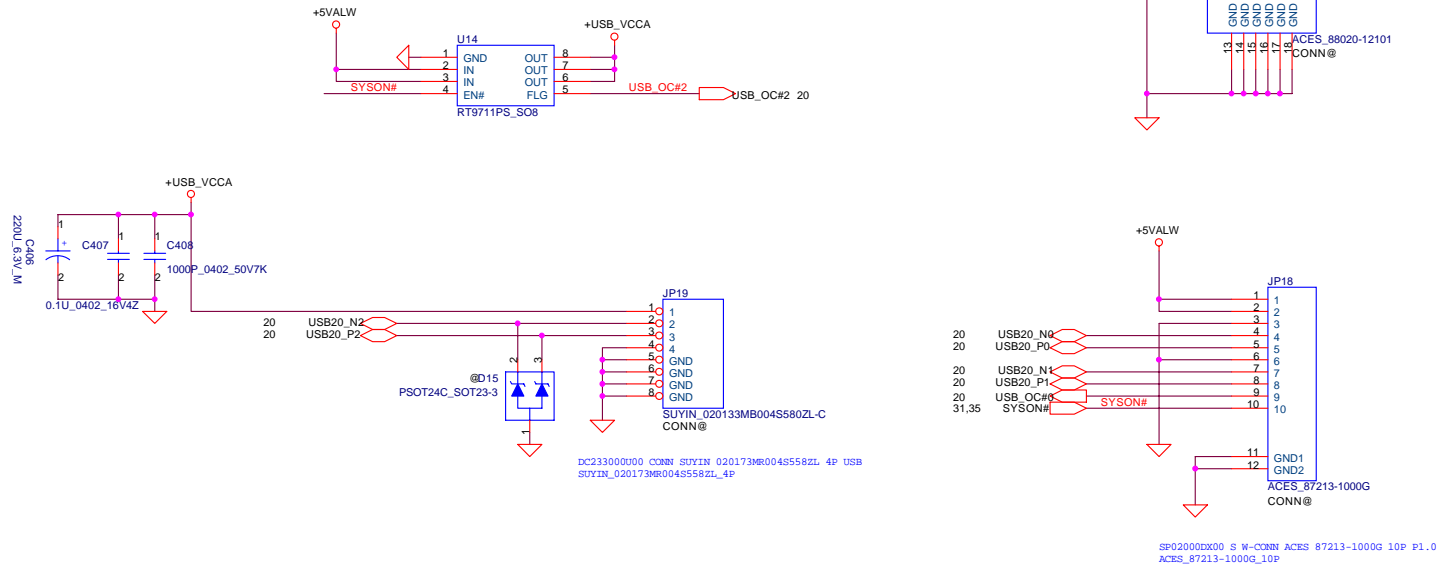


Revision History

REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

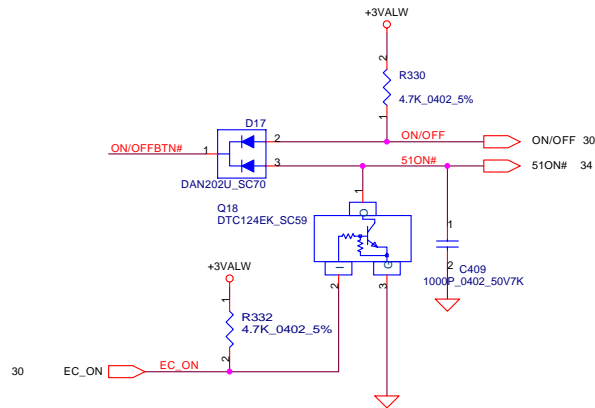
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				Size	Document Number	Rev
					LA-3732P	1.0
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USB Port

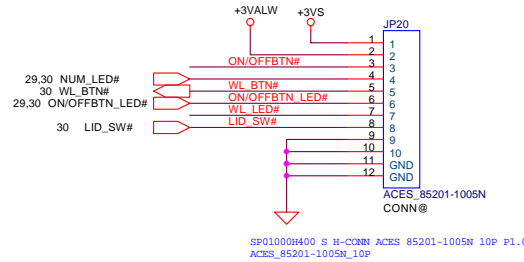


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				USB CONN.			
Size		Document Number				Rev	
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Power ON/OFF

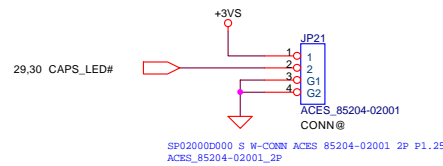


M/BtoS/B

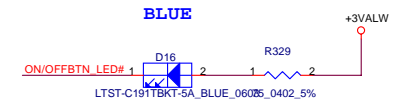


0426_Change all LED power source from 5V to 3V.

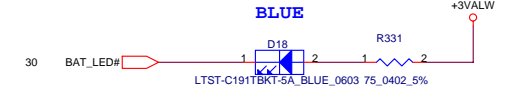
M/B to SB(Caps Lock LED)



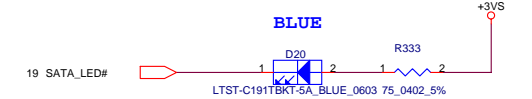
POWER LED(Left 1)



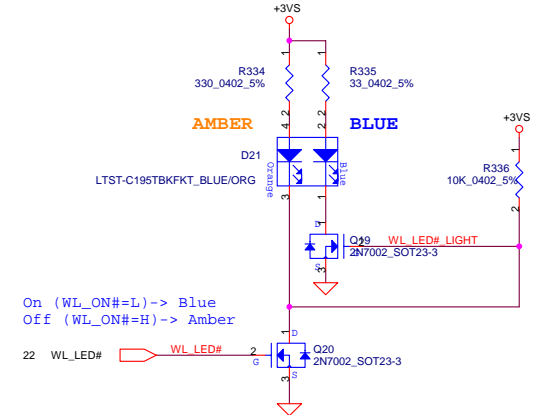
Battery Charge LED(Left 2)



HDD LED(Left 3)



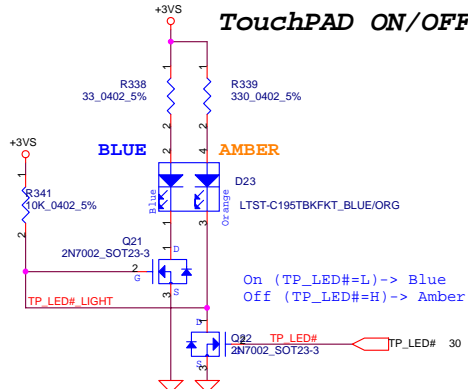
Wireless ON/OFF LED(Left 4)



On (WL_ON#=L) -> Blue
Off (WL_ON#=H) -> Amber

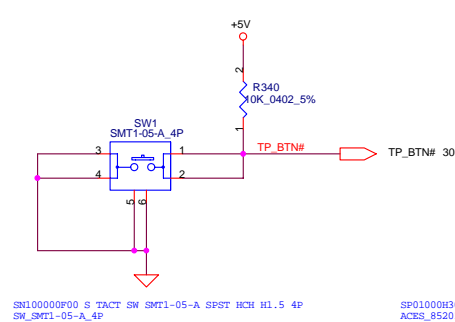
D21, D25, D23 Footprint can not match part number.

TouchPAD ON/OFF LED

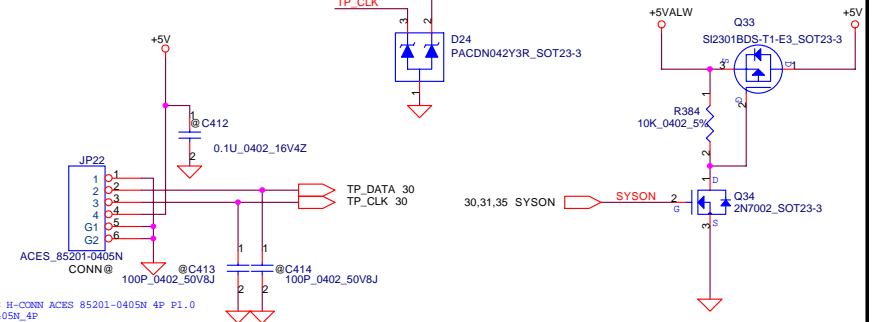


On (TP_LED#=L) -> Blue
Off (TP_LED#=H) -> Amber

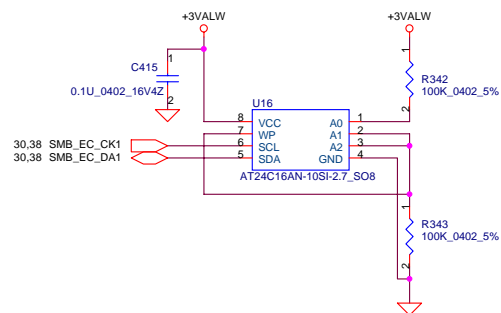
TP ON/OFF



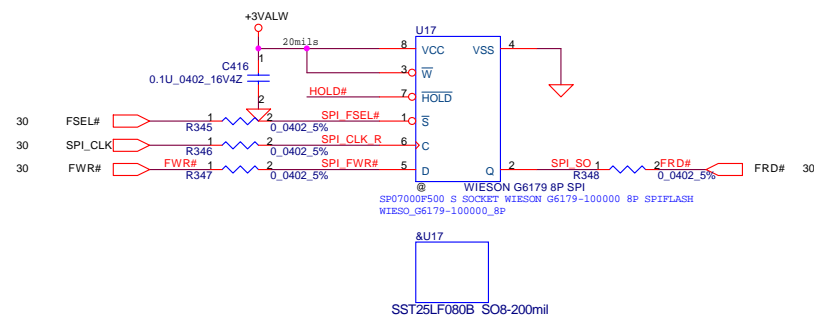
T/P Board



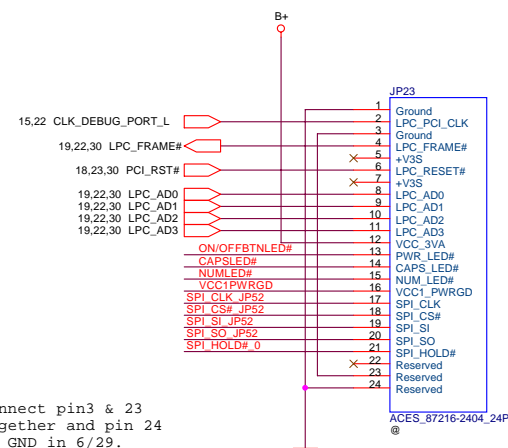
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				Size Document Number
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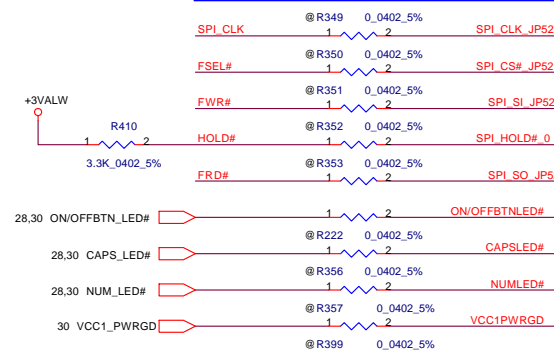
SPI ROM



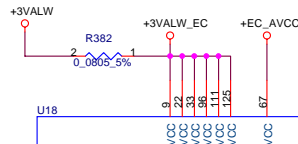
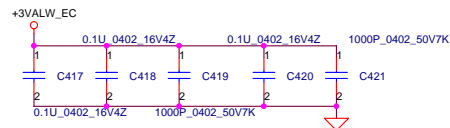
LPC Debug Port



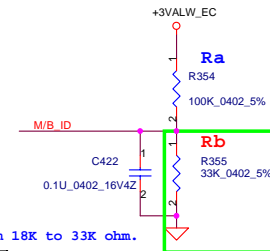
Connect pin3 & 23
together and pin 24
to GND in 6/29.



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Size		Document Number		Rev	
		LA-3732P		1.0	
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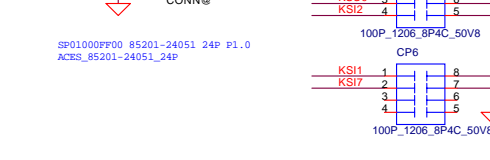
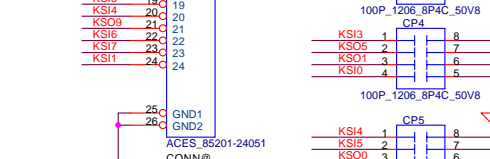
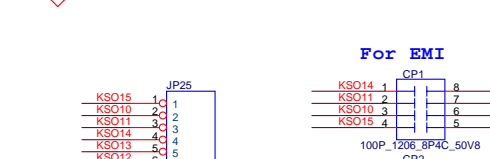
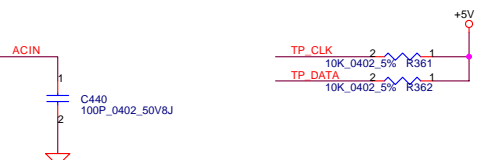
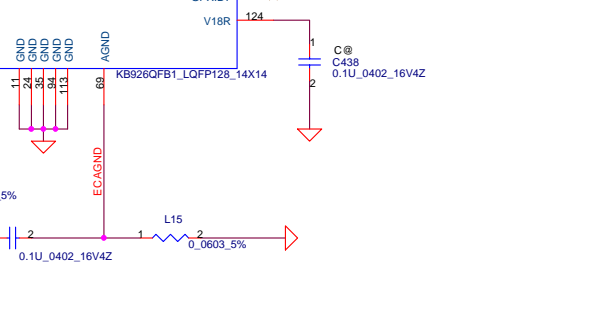
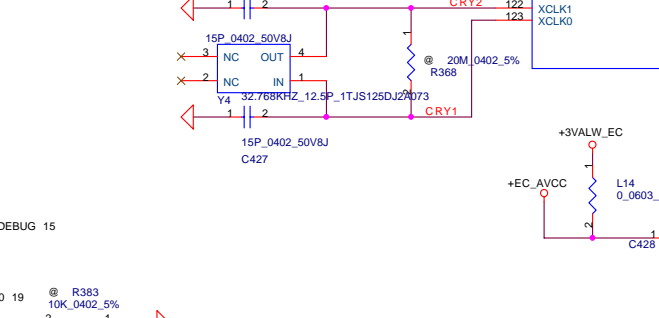
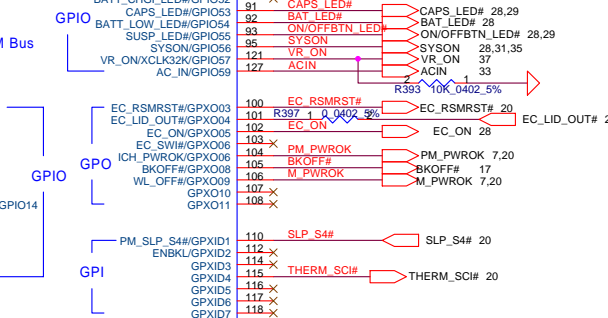
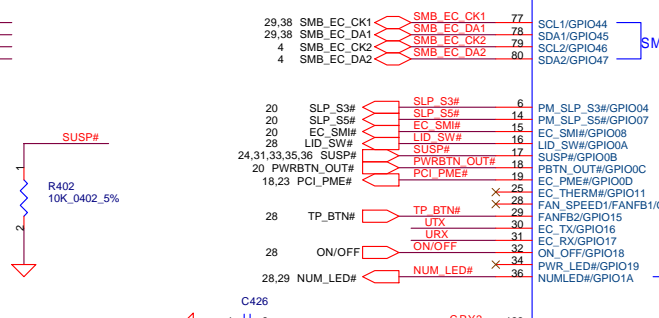
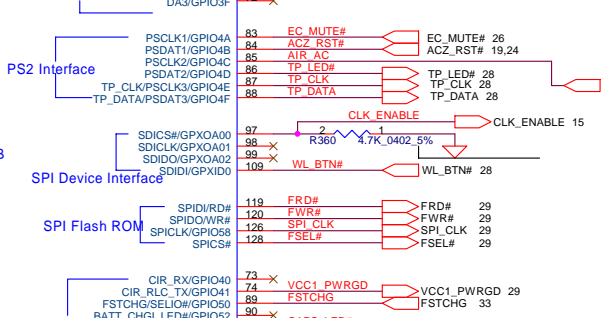
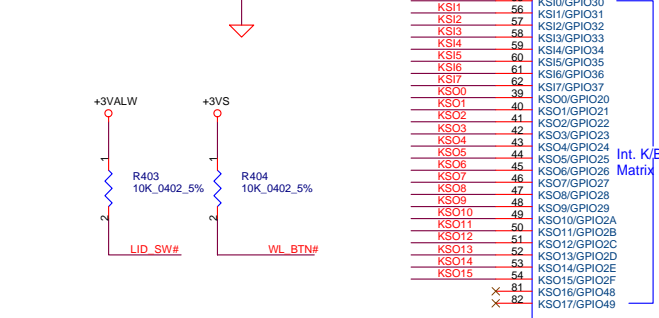
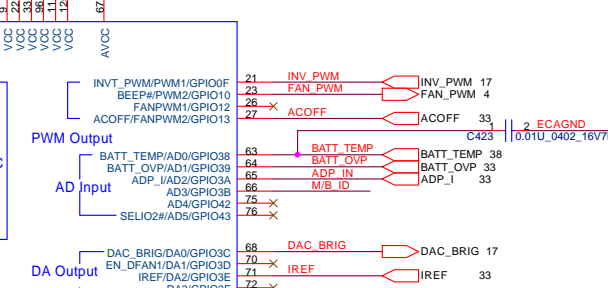
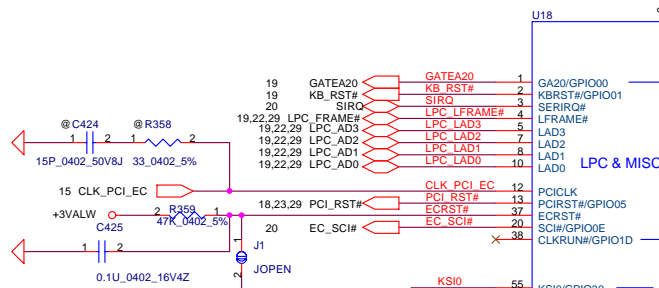


Board ID
DB : 0
SI : 1
PV : 2
MV : 3



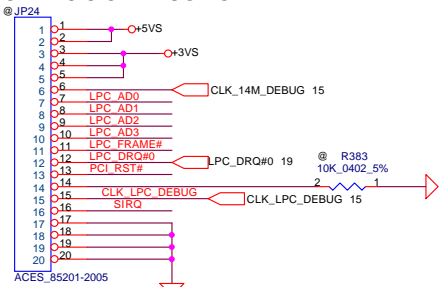
0605_Change R355 from 18K to 33K ohm.

VCC	3.3V+/-5%				
Ra	100K+/-5%				
Board ID	Rb	V _{AD_STD} min	V _{AD_STD} typ	V _{AD_STD} max	
0	0	0V	0V	0V	
1	8.2K+/-5%	0.216V	0.250V	0.289V	
2	18K+/-5%	0.436V	0.503V	0.538V	
3	33K+/-5%	0.712V	0.819V	0.875V	
4	56K+/-5%	1.036V	1.185V	1.264V	
5	100K+/-5%	1.453V	1.650V	1.759V	
6	200K+/-5%	1.935V	2.200V	2.341V	
7	NC	2.500V	3.300V	3.300V	



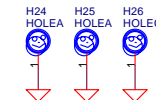
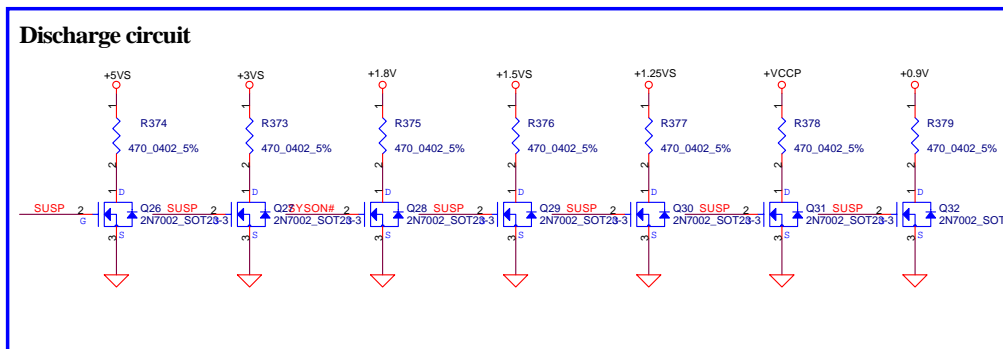
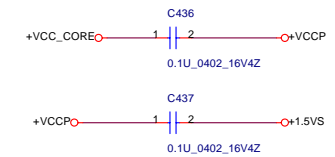
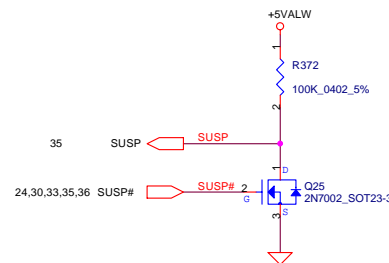
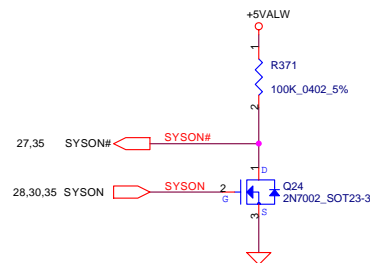
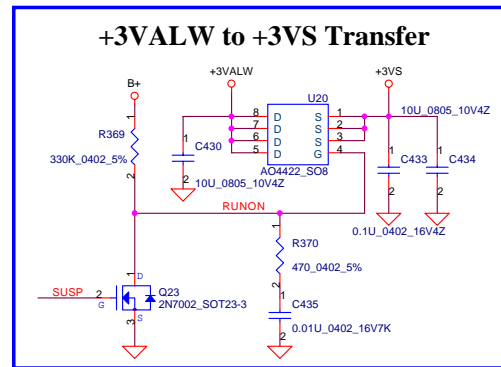
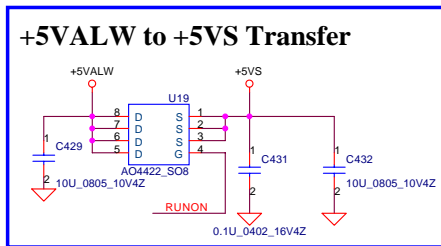
EC DEBUG port

FOR LPC SIO DEBUG PORT

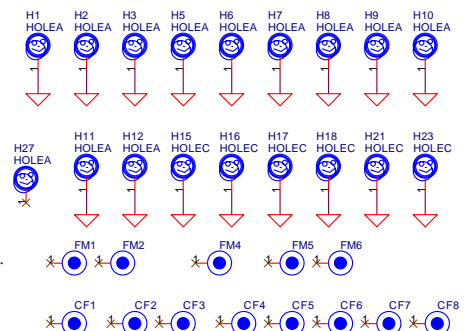


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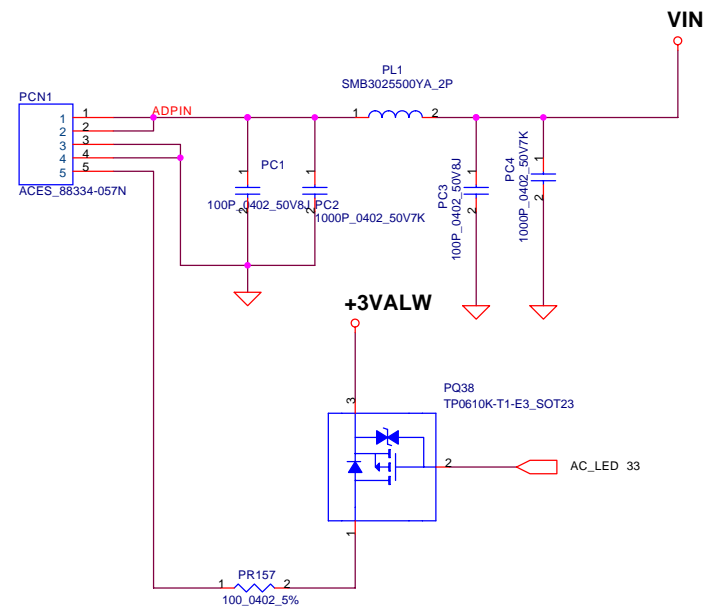


For Card reader/B stand off.

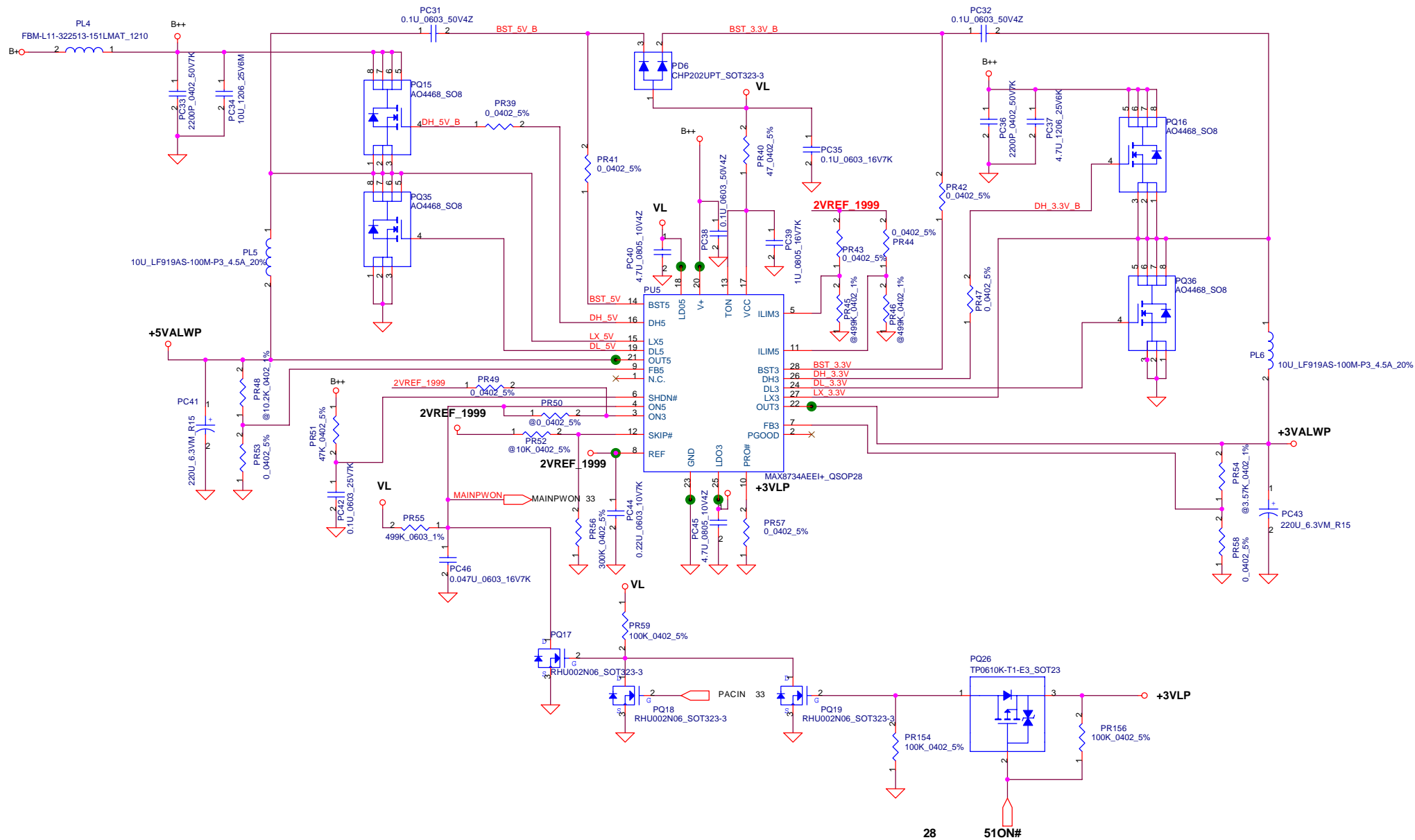


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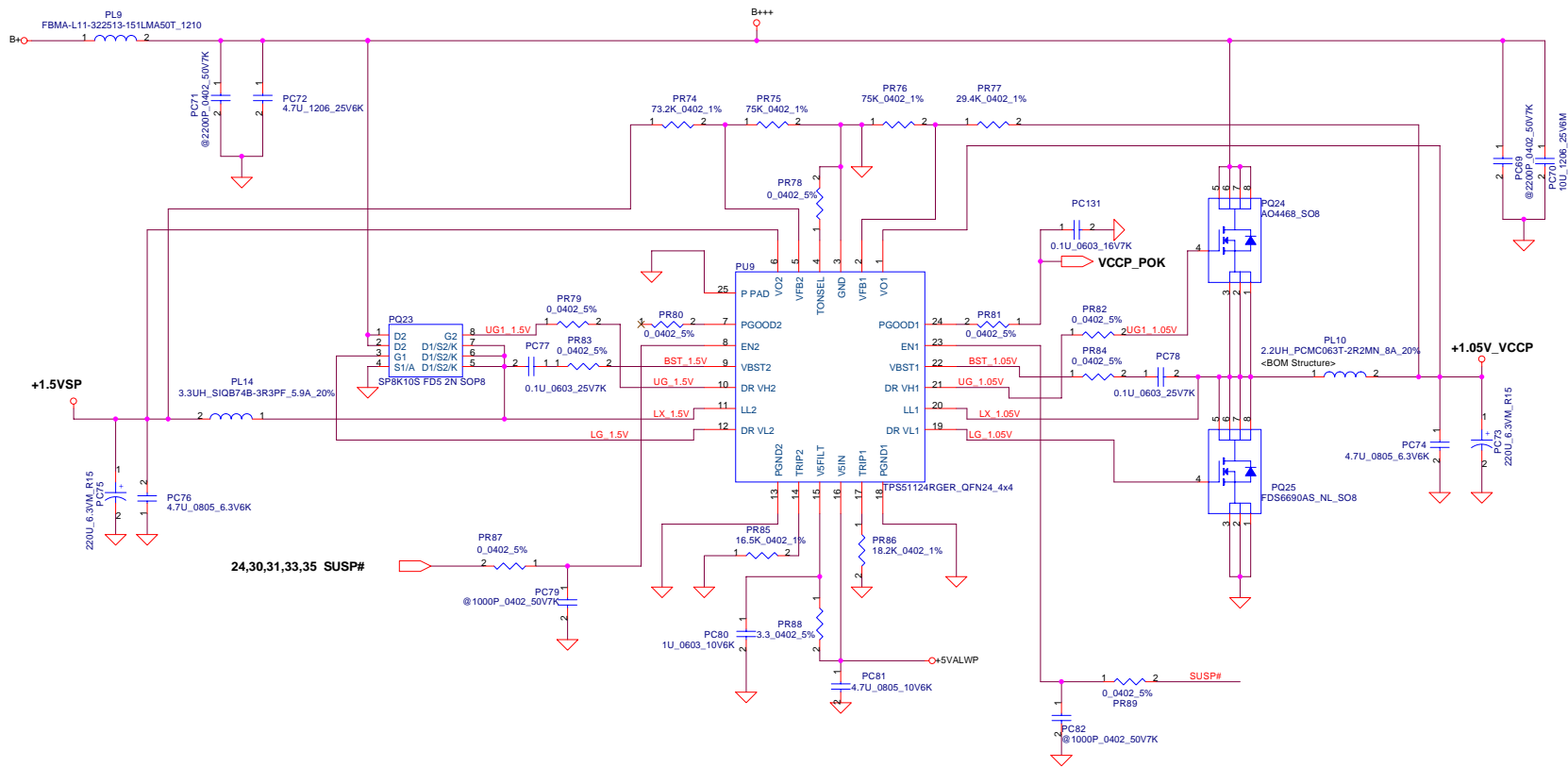


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				Size	Document Number	Rev
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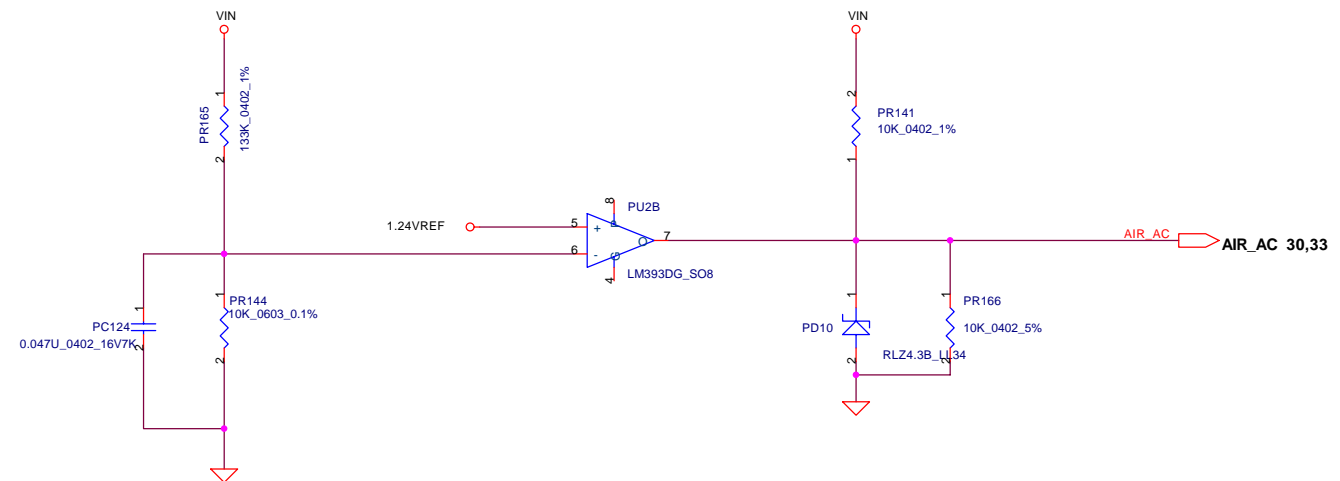
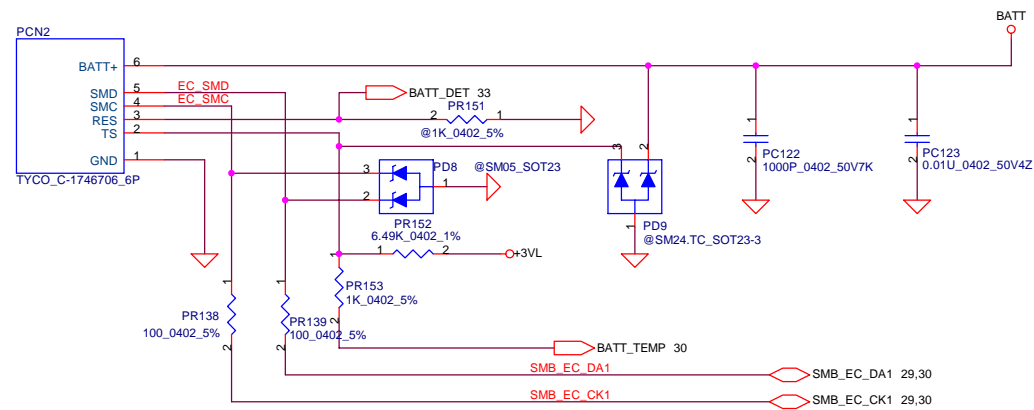
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Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>	Title	
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24,30,31,33,35 SUSP#

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Item	Change item	Page	Date	Phase
1	Change C117 from 220uF to 10uF.	10	2/8	DB --> SI
2	Remove R401.	19	2/5	DB --> SI
3	Change Crystal Y2 type (the same as Abita).	19	2/5	DB --> SI
4	Connect LAN_RST# from EC_RAMRST# to GND.	20	2/5	DB --> SI
5	Change ODD connector type.	22	2/13	DB --> SI
6	Change U11 power from +5VS to +5VALW.	24	2/12	DB --> SI
7	Change U11 enable signal from SLP_S3# to SUSP#.	24	2/8	DB --> SI
8	Reverse JP19 USB Connector and need to double check layout symbol.	27	2/12	DB --> SI
9	Change Power and Battery charge LED power from +3VALW to +5VALW.	28	2/8	DB --> SI
10	Change HDD LED power from +3VS to +5VS.	28	2/8	DB --> SI
11	Delete reserve component (D25 BSW2) for 14.1".	28	2/8	DB --> SI
12	Change R329, R333, R470 from 200 ohm to 470 ohm.	28	2/8	DB --> SI
13	Change R334, R339 from 200 ohm to 820 ohm.	28	2/8	DB --> SI
14	Add pull down resistor R402 (100k ohm) for SUSP#.	30	2/5	DB --> SI
15	Change C44, C49 type from DIP to SMD.	06	2/14	DB --> SI
16	Add R402 pull high resistor for LID_SW#.	30	2/14	DB --> SI
17	Add R403 pull high resistor for WL_BTN#.	30	2/14	DB --> SI
18	Delete D19.	28	2/16	DB --> SI
19	Change R300 from 10 ohm to 47 ohm and C374 from 10pF to 33pF.	24	2/16	DB --> SI
20	Delete JP27, R317, C392.	26	2/16	DB --> SI
21	Delete R297.	24	2/16	DB --> SI
22	Change RTC battery and connector.	19	2/26	DB --> SI
23	Change C413 and 414 package from 0603 to 0402.	28	2/26	DB --> SI
24	Add JP28 for USB card reader.	27	2/28	DB --> SI
25	Change R105 from 22 ohm to 0 ohm.	15	3/1	DB --> SI
26	Delete C49 and remount C46.	06	3/1	DB --> SI
27	Change JP16 and JP17 Audio Jack.	26	3/2	DB --> SI
28	Add R405.	04	3/6	DB --> SI
29	Change USB connector (JP19) type.	27	3/8	DB --> SI

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Item	Change item	Page	Date	Phase
1	Connect R323.1 from B+ to +3VALW. (Cancel in 4/24)	26	4/9	SI --> PV
2	Add R406 between H_OUT_R and H_OUTR+, R407 between H_OUT_L and H_OUTL+	26	4/9	SI --> PV
3	Swap channel L and R.	26	4/9	SI --> PV
4	Add R408 and R409. (Cancel in 4/24)	26	4/9	SI --> PV
5	Reverse JP22 pin define.	28	4/10	SI --> PV
6	Change R360 from 10K to 4.7K ohm for KB926 C0 version.	31	4/10	SI --> PV
7	Reserve C438 for KB926 C0 version.	31	4/10	SI --> PV
8	Change C45~C48 to 9m ohm and reserve C49.	06	4/16	SI --> PV
9	Change R233 from 0 ohm to 10K ohm.	20	4/16	SI --> PV
10	Change R233 from 0 ohm to 10K ohm.	30	4/16	SI --> PV
11	Reverse JP15 pin define.	26	4/16	SI --> PV
12	Add pull high R410 (3.3K ohm) for HOLD#.	29	4/17	SI --> PV
13	Change R211 from 24.9 to 27.4 ohm.	19	4/17	SI --> PV
14	Add CPL~CP6 for EMI.	30	4/17	SI --> PV
15	Add R186 and C261 for EMI.	18	4/17	SI --> PV
16	Add R292 and C356 for EMI.	23	4/17	SI --> PV
17	Add D24 for EMI.	28	4/17	SI --> PV
18	Add C233, C234, C235 for EMI.	16	4/17	SI --> PV
19	Add R411 to pull high for WL_LED#.	22	4/17	SI --> PV
20	Remove XDP circuit for EMI request. Change R2 to 15 ohm R3 to 39 ohm R7 to 560 ohm R8 to 27 ohm	04	4/17	SI --> PV
21	Change R223 from 1K to 10K ohm when remove XDP.	20	4/17	SI --> PV
22	Add reserve resistor R412 for LPC debug port.	15	4/17	SI --> PV
23	Add C439 to avoid wavelike display.	10	4/20	SI --> PV
24	Change C262 and C263 from 15pF to 12pF.	19	4/23	SI --> PV
25	Per ENE request, change C426 and C427 from 10pF to 27pF from now.	30	4/23	SI --> PV
26	Reserve R300 and C374 for EMI request.	24	4/24	SI --> PV
27	Add C440 for AC_IN.	31	4/24	SI --> PV
28	Change R355 from 8.2K to 18K ohm.	31	4/25	SI --> PV
29	Add L16~19 for EMI request.	26	4/25	SI --> PV
30	Change C336~C338 from 22p to 10pF.	16	4/25	SI --> PV
31	Add R415 and R416 for thermal second solution.	04	4/25	SI --> PV
32	Change R320 from 0 ohm to bead. Add L20.	26	4/25	SI --> PV
33	Change R321 and R322 from 0 ohm to bead. Add C398 and C399.	26	4/25	SI --> PV
34	Add C401 and C404.	26	4/25	SI --> PV
35	Connect AIR_AC to U18 pin85 to support AIR adapter.	31	4/26	SI --> PV
36	Add C441.	15	4/26	SI --> PV
37	Add R417 and R418 to fine tune Headphone output voltage	26	4/26	SI --> PV
38	Delete R219 and C268 for EMI request.	20	4/26	SI --> PV

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